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# Design of Operational Transconductance Amplifier with High Gain

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***Abstract-*** **In recent years interests have been seen in wireless system and software radio using sigma-delta modulators to digitize signals near the front end of radio receivers. Such applications necessitate clocking the modulators at a high frequency (MHz or above). A continuous-time implementation using transconductors and integrators rather than discrete time implementation using switched capacitors is preferred for high frequency operation. A novel cross coupled operational transconductance amplifier (OTA) has been developed with high linearity at high frequency which can be used in design of continuous time sigma delta modulator. The proposed cross coupled OTA achieves gain of 35dB, third order Intermodulation (IM3) of -73dB at a high frequency range of 70 MHz with an effective Transconductance of 3.34mA/V. The proposed OTA is implemented in 180nm CMOS technology**

***Keywords--*** **Analog and Mixed Signal IC Design, OTA, Linearization, Source Degeneration and Cross Coupling**

## I. INTRODUCTION

Filter which will be implemented using an OTA – C topology. Hence the most important part of the modulator is the OTA. The main specifications of loop filter are very high linearity, high tuneablility and high DC-gain [1]. The minimum input of the modulator is determined by the input referred noise seen at the transconductor, and the maximum input is limited by the linearity of transconductor, because transistors have nonlinear behavior at high frequency and introduce harmonic distortions [2]. To a large extent, the dynamic range of overall modulator is determined by the input transconductor. The distortion of the other transconductor in the design flow will generate in band noise and also degrade the SNDR and DR of modulator [3]. Therefore, the transconductor needs to be highly linear.

**Table 1:**
**Specifications of proposed OTA**

| OTA parameters | Values |
|---|---|
| DC-gain | 35dB |
| Gm | 3.34mA/V |
| IM3 at 70MHz | -73dB |

## II. OTA DESIGN

This paper will focus on the design of operational transconductance amplifier (OTA). The performance of the sigma delta modulator is governed by the loop. The simplicity and linearity are the essential features of the OTA intended for any application. Large transconductances are needed for the bandpass resonator operating at 70 MHz, and their implementation usually employs large-dimension transistors and tail-current. However, transistors with large size introduce parasitic poles at lower frequencies. The use of large tail current will also increase the power consumption and further reduce the DC gain of transistors [4]. A general differential pair has a good frequency response due to the absence of low-frequency parasitic poles. The problem of this topology is that the DC gain is very limited. Cascode output stages can boost the gain but introduce parasitic poles at the cascode node. An efficient OTA based on the complementary differential pairs was reported in [9], and is shown Figure 2.When compared with op-amps OTA's are much faster and does not suffer from bandwidth and slew rate requirements.There are various types of linearity techniques like source degeneration using resistors, cross coupling techniques and so on.This paper combines both the techniques to improve linearity and gain of the operational transconductance amplifier.

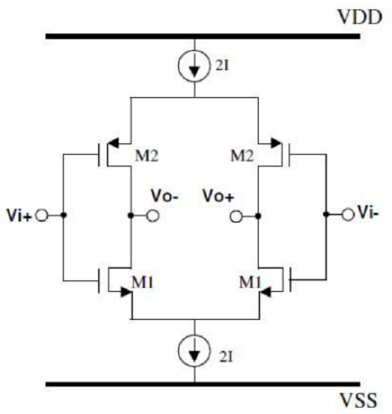

**Figure 2: Differential amplifier based OTA**

The OTA uses two differential pairs M1 and M2 as the driving stage, and both differential pairs draw from the same tail current. The effective transconductance increases but the power consumption is not increased. One part of the differential output current comes from N-type pairs M1, and the other from P-type pairs M2. With the help of small-signal transistor model, the effective OTA transconductance is given by,

$$Gm=gm1+gm2 \tag{1}$$

Where gm1 and gm2 are small-signal transconductances of M1 and M2, respectively. There are several circuit techniques reported with improved linearity of MOS transconductors. Most commonly used linearization methods are nonlinear term cancellation, attenuation and source degeneration [1]. Nonlinear term cancellation is realized by means of optimal algebraic sum of nonlinear term. However the linear range is very restricted and a good cancellation is hard to achieve [10]. In the attenuation technique, the input voltage is reduced or attenuated by several factors in magnitude to improve the linearity. The drawback is that a higher gain is required to compensate the input attenuation, resulting in large area and more power consumption. Compared to the two techniques, source degeneration is a technique mostly employed.

## III. LINEARIZATION TECHNIQUES

The difference between the two structures is how the current source is connected. Structure 2(a) has higher common-mode voltage swing at input. Also the noise contributed by current source is injected to a single output and appears like differential noise at the output node.

In structure 2(b), the noise goes through the two branches evenly, and looks like common-mode noise.

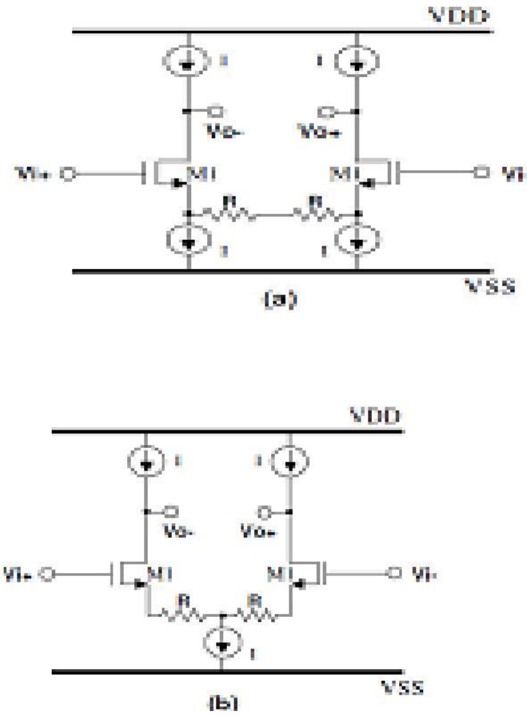

**Figure 3(a): Source degeneration using separate current sources.**
**Figure3 (b): Source degeneration using same current source**

## IV. IMPLEMENTATION OF SOURCE DEGENERATION

The proposed cross coupled OTA combines both techniques reported in [4], [3] and [2].[4] uses source degenerated OTA and has IM3 of -62dB,dc gain of 14dB and Unity gain frequency of 4.7GHz and is shown below in figures 2.3,2.4 and 2.5.In order to evaluate the gain of OTA using source degeneration[4] AC analysis is performed in cadence to obtain gain.PSS analysis is performed by applying two tone signal test of 70MHz and 71MHz to obtain Intermodulation product(IM3).

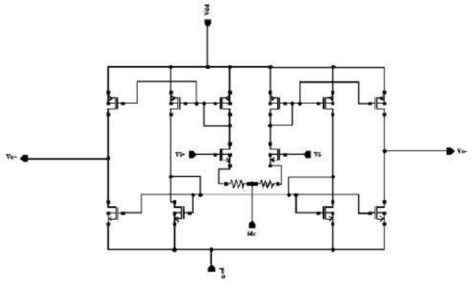

**Figure 4.1: OTA using source degeneration [4]**

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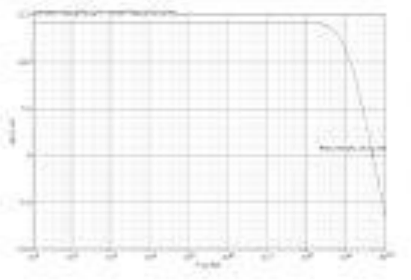

**Figure 4.2: Response of AC analysis showing gain and UGB**

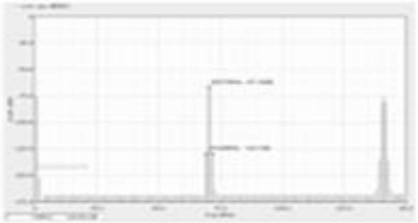

**Figure 4.3: Response of pss analysis for a two tone test**

The proposed OTA is shown below. source degeneration and cross-couple cancellation are employed to achieve a high linearity.

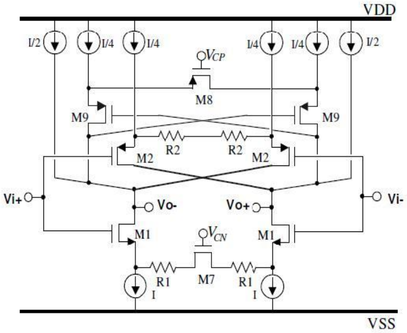

**Figure 4.4: Proposed OTA**

Current sources are implemented by transistor M3, M4 and M5. The dimensions of M5 (M6) are three times the size of M4 (M2) to provide M2 the proper bias current and reduce the mismatch. A power supply of1.8 V is used so there is some headroom for the structure. Poly-poly resistors, instead of transistors, are used to implement source degeneration resistors because of small resistance and the nonlinearity of active elements.

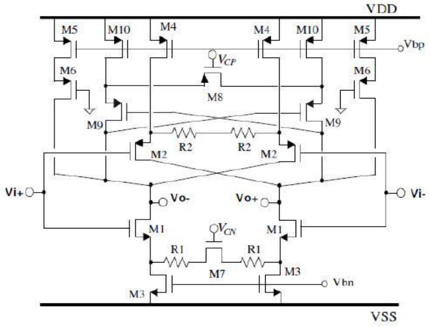

**Figure 4.5: Complete OTA structure**

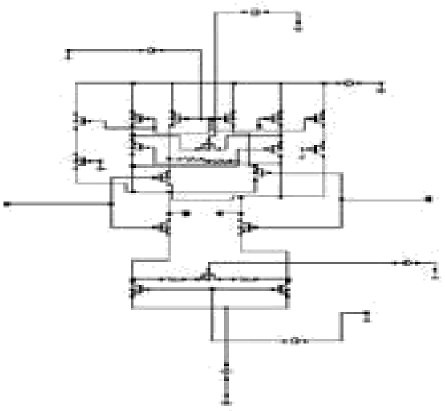

**Figure 4.6: Schematic of proposed OTA**

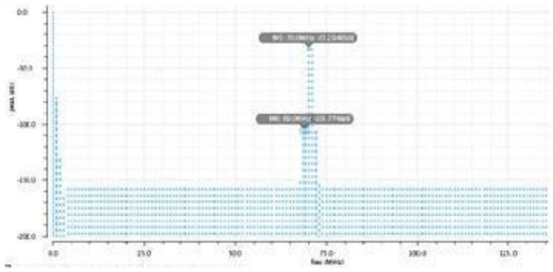

**Figure 4.7: PSS analysis to calculate IM3**

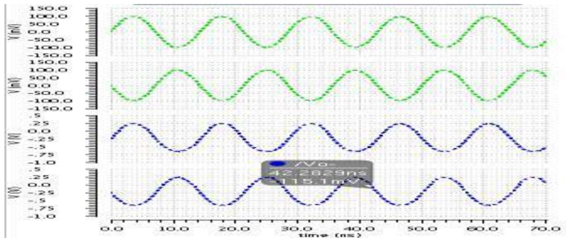

**Figure 4.8: Transient analysis of proposed OTA**

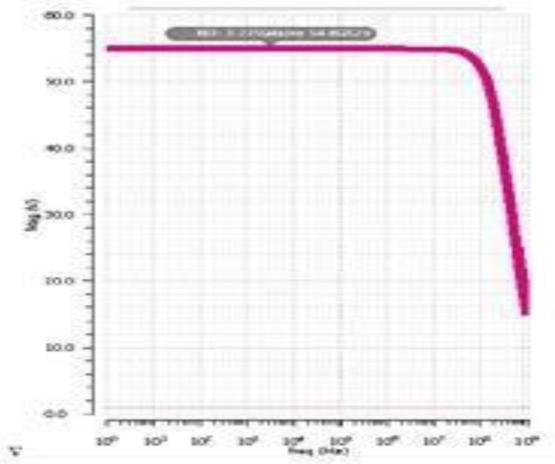

**Figure 4.9: Gain of proposed OTA**

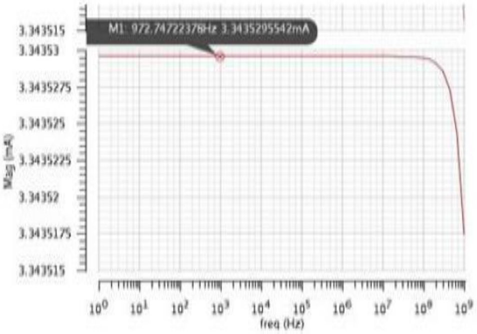

**Figure 4.10: Transconductance of proposed OTA**

## V. CONCLUSION

The Performance Comparison of source degenerated OTA [4] and Proposed OTA is shown in table 2. It can be seen that the gain has increased by 19dB and IM3 is almost same.UGB of proposed OTA has reduced to 1.2GHz. The proposed OTA can be used in the design of continuous time loop filter which is the most important block of sigma delta modulator [6]

**TABLE 2:**
**Performance Comparison of source degeneration OTA [4] and proposed OTA**

| **OTA parameters** | **Source degenerated OTA[4]** | **Proposed OTA** |
|---|---|---|
| DC Gain | 14dB | 34.1dB |
| Unity Gain Bandwidth | 4.76GHz | 1.2GHz |
| Effective Transconductance Gm | 655.8uA/V | 3.34mA/V |
| Third Order Intermodulation(IM3) | -62dB | -73dB |

frequency compensation scheme".IEEE.trans. circuits and systems brief II,vol 53,pg.797-801,sep 2010.s

## REFERENCES

[1] J.silva-Martinez and E.sanchez,"CMOS transconductance amplifiers, architectures and filters:a tutorial",in IEEE proceedings on circuits ,devices,vol.147,Feb 2007.pp 3-12.

[2] J.silva-Martinez and Lewinksi",OTA linearity enhancement technique for high frequency application",CICC 2007,sept 2007 pp 3-12

[3] J.silva Martinez and b.Nauta "A CMOS transconductance filter technique for very high frequencies",IEEE solid state circuits,vol 27,Feb 2012,pp 142-153

[4] Mohammed Arifuddin Sohel,Dr.Kchennakeshava reddy,Dr.Syed Abdul Sattar,"Linearity enhancement of operational transconductance amplifier using source degeneration",Vol.4,April 2013,pp-257-263

[5] Richard schrier,M.Snelgrove,"Bandpass sigma delta modulation",IEEE electronics letter,vol.25,2008,pp.1560-1561.

[6] Richard schrier ,G.temes,"Understanding sigma delta modulators",MJ.wiley,IEEE press 2005

[7] B.Razavi,"principles of data conversion system design",New York,IEEE press 2005

[8] 8.P.R Gray,P.J Hurst,S.H Lewisand R.J Meyer,"Analysis and design of Analog Integrated Circuits",Newyork,wiley:2001.

[9] T.Lin,C.Wu,"A current mirror OTA with 160MHz GBW in 0.18um CMOS",IEEE trans.Circuit and systems,vol.54,pg 131-135,feb

[10] F.A.P Baruqui,A.Petralgia,"Three stage CMOS OTA with large capacitive loads with efficient

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