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# Implementation of Dynamic Switching Type Signal Generation on FPGA for Navigation Receivers

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***Abstract*— The important role in navigation test, radio navigation generator is widely used in the people/military plane. Modulation switching is the main concept in this paper. In the previous we are using only AM modulation type of testing the navigation receivers. But todays communication systems use more than one modulation technique. So a new kind of digital navigation signal generator is designed that supports several modulation techniques. Those are AM, FM, BPSK, QPSK. So depends upon our requirement we are automatically switching from one modulation technique to another modulation technique. Therefore, in this paper a new idea is provided for radio navigation system design and test. This signal generator can be widely applied to debugging use of people/military plane radio navigation.**

***Keywords*— ADC, DAC, DDS signal generator, FPGA (Spartan-3E), Microblaze, Navigation.**

## I. INTRODUCTION

In modem aviation, navigation is an important technology. So far, equipped in almost all the military and civil airports, radio navigation system is the most widely used navigation devices in aviation. At present, radio navigation still has priority in short-range navigation of civilian and military aviation in our country. Also, due to the imperfect landing system device in the existing aircraft, radio navigation system is of vital importance in ensuring safety in plane's homing and approaching [1].

In the actual navigation test, to simulate the RF signal of combined antenna in radio navigation, various signal generators are often designed to satisfy performance of navigation system and meet technical requirements. Meanwhile, the signal generator must adjust signal types, parameters and work modes timely according to the navigation system requirements[2]. Therefore, signal generator must have the feature that signal can be generated flexibly, parameters change quickly, signal spectrum stay stabilized, and the system is reliable, etc.

The proposed system adopts Micro Blaze soft processor[3]-[4] as the control core of generator to communicating command with PC. Which can satisfy each requirement in actual application of testing and debugging on navigation[5].The important role in navigation test, radio navigation generator is widely used in the people/military plane. But traditional equipment composed of analog circuit Presents low accuracy and poor reliability. A new kind of digital navigation signal generator is designed. It receives data and commands from PC by MicroBlaze embedded soft processor of Xilinx company and demodulates information to control FPGA load different softwares to generate various navigation signals, which fully meets general radio navigation system test technical requirements by giving full play to the system hardware and software advantages and fulfilling design targets such as the accuracy, flexibility and expansibility. Therefore, providing a new idea for radio navigation system. this generator can be widely applied to debugging use on people/military plane radio navigation.

The reference paper implements only AM modulation type for testing the navigational receivers.

- But today's communication systems use variety of latest digital modulation techniques, hence we have developed two architectures one for analog and other for digital modulations in this project.
- For realizing the digital modulation we have used Universal digital modulator for generating all type of digital modulated signals.
- signal generator will be designed that contains feature that signal can be generating flexibly, parameters change quickly, signal spectrum stay stability, and the system is reliable, etc.
- Fundamentally, characteristics of signal patterns and real-time variability are mainly embodied in signal generation technology.

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- This system adopts MicroBlaze soft processor as the control core for generating communicating command with PC and controlling FPGA load different softwares to synthesize various navigation signals.

Here we are implementing AM, FM, BPSK, QPSK modulation techniques.

## II. Direct Digital Synthesizer & Processing Modules

According to different technical requirements of navigation, the generated signal is basically formed by the carrier signal, low frequency modulated signal and audio modulated signal. Therefore, in this scheme, the signal generator adopts direct digital frequency synthesizer (DDS) technology to design precise clock reference source, word length of frequency and phase accumulator and sine function table to generate the modulated sine signal whose frequency variation scope, step length change and precision meet the acquirements in overall design. Large-scaled FPGA is used in this system to realize accurate DDS.

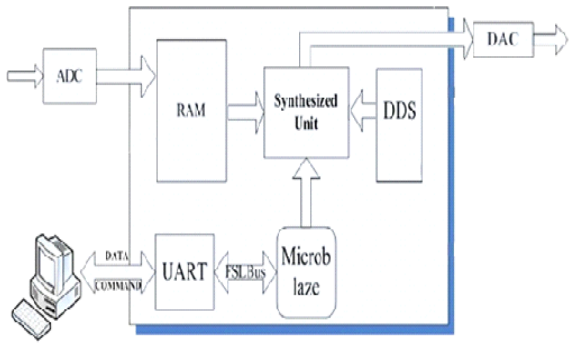


**Figure 1. Processing modules of FPGA**

Figure 1 shows the block diagram. It consists of

- *ADC:* Used for converting analog signals to digital values. Mainly used for formation of bits.
- *RAM:* Used for storing the digital values.
- *Microblaze:* Is a softcore processor used to give commands.
- *UART:* Serial cable interface used for communication purpose. It translates the data between parallel and series forms.
- *Synthesized unit:* Consists of all 4 modulation techniques. It is used for selecting the modulation technique.
- *DDS:* Used for generating high frequency carrier signal.
- *DAC:* Used for converting digital signal to analog signal.

ADC converter is used to convert the external signal to be modulated by carrier signal, and the soft embedded processor MicroBlaze communicates with PC by RS422/232 as the control core, figure 1 is the overall scheme of digital signal generator of radio navigation. The control software of PC wrote in VC6.0 communicates with the generator through RS422/232 is in charge of transmitting control command to set frequency, azimuth angle, channel, working mode and other parameters of navigation signal and receiving status and data of the generator after every change. In this system, as a master unit MicroBlaze sends parameters to FPGA after demodulating data from PC while FPGA generates accurate navigation signal to high-speed DAC converter as the ground floor synthesis unit. Meanwhile, multiple clock signals used in the system are generated in phase lock logic part of FPGA from external oscillator.

### *A. DDS*

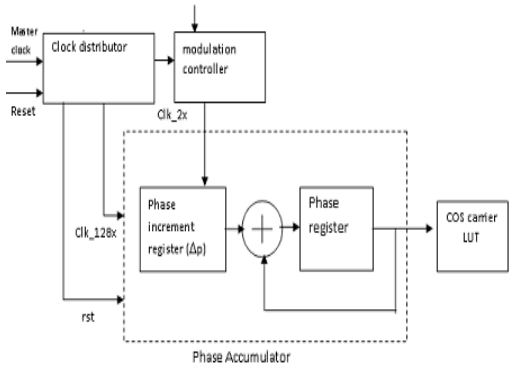


**Figure 2. Direct Digital Synthesizer**

A Direct Digital frequency Synthesizer (DDS) design and prototype suitable for space-borne applications is presented. The design is targeted for use in the uplink section of the RF subsystem of the New Horizons Pluto spacecraft currently under design at APL. Design and analysis of the digital portion of the DDS is presented along with experimental data from the prototype system, which was implemented using an FPGA and a discrete digital to analog converter.

Direct Digital frequency Synthesizers (DDS) are a common component in a variety of communication systems, especially those requiring fast frequency hopping, low power dissipation, and small form factor.

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*1) Implementation of DDS:* In this project we are using Direct Digital Synthesizer for generation of the carrier signal. All we know about that by using DDS we can generate a carrier signal in the form of sine or cosine or sinecosine. Xilinx itself generate the core for DDS that is IP Core generation. In that we should select options about the carrier or signal frequency in MHZ and phase off set and data width and the phase increment register data width depends on the data width or we can have a option like programmable then we can give the phase of set and frequency levels through the program.

And we are taking the carrier signal from the DDS and we do the modulation like AM,FM,QPSK,BPSK.And in FM technique we are taking DDS signal as the message signal and we are generating the carrier by using the Hardware Description Language.

*B. ADC*

The Analog to Digital Module Converter Board (the AD1™) converts signals at a maximum sampling rate of one million samples per second, fast enough for the most demanding audio applications. The AD1 uses a 6-pin header connector, and at less than one square inch is small enough to be located at the signal source.

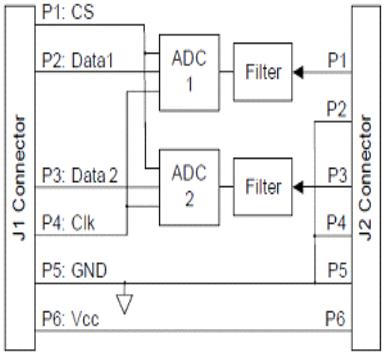


**Figure 3. ADC Circuit Diagram**

The AD1 converts an analog input signal ranging from 0-3.3 volts to a 12-bit digital value in the range 0 to 4095. The AD1 has two simultaneous A/D conversion channels, each with a 12-bit converter and filter. Each channel can sample a separate stream of analog signals. The AD1 can also convert a single stream of analog signals using only one channel. Each channel has two 2-pole Sallen-Key antialias filters with poles set to 500 KHz. The filters limit the analog signal bandwidth to a frequency range suitable to the sample rate of the converter. The AD1 uses the SPI/MICROWIRE™ serial bus standard to send converted data to the host system.

The serial bus can run at up to 20 MHz. The AD1 has a 6-pin header and a 6-pin connector for easy connection to a Digilent system board or other Digilent products. Some system boards, like the Digilent Pegasus board, have a 6-pin header that can connect to the AD1 with a 6-pin cable. To connect the AD1 to other Digilent system boards, a Digilent Modular Interface Board (MIB) and a 6-pin cable may be needed. The MIB plugs into the system board, and the cable connects the MIB to the AD1. The AD1 can be powered by voltage from either a Digilent system board or an outside device. Damage can result if power is supplied from both sources or if the outside device supplies more than 3V.

*C. DAC*

The Digilent PmodDA2 Digital to Analog Module Converter, converts signals from digital values to analog voltages on two channels simultaneously with twelve bits of resolution. The PmodDA2 uses a 6 pin header connector and, at less than one square inch, is small enough to be located where the reconstructed signal is required.

The PmodDA2 can produce an analog output ranging from 0-3.3 volts when operated with a 3.3V power supply. It has two simultaneous D/A conversion channels, each with a 12-bit converter that can process separate digital signals.

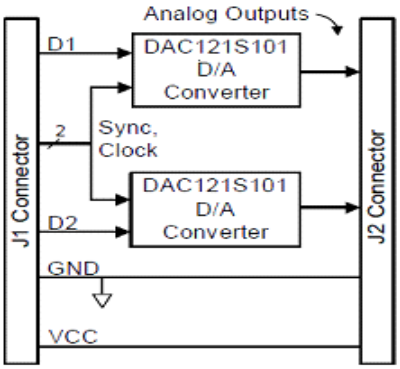


**Figure 4. DAC Block Diagram**

The PmodDA2 is equipped with two DAC121S101 digital to analog converters. Sending commands via the SPI/MICROWIRE™ serial bus to the D/A converters produces outputs. The two converters are connected in parallel so that commands are sent to both converters simultaneously. The PmodDA2 is designed to work with either Digilent programmable logic system boards or embedded control system boards.

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Most Digilent system boards, such as the Nexys, Basys, or Cerebot, have 6-pin connectors that allow the PmodDA2 to plug directly into the system board or to connect via a Digilent six-wire cable Some older Digilent boards may need a Digilent Module Interface Board (MIB) and a 6- pin cable to connect to the PmodDA2. The MIB plugs into the system board and the cable connects the MIB to the PmodDA2.

Below Table shows the description of the signals on the interface connectors J1 and J2.

**TABLE I**
**INTERFACE CONNECTOR SIGNAL DESCRIPTIONS**

| **Digital Interface – J1** | |
|---|---|
| 1 | SYNC (common) |
| 2 | DINA (converter IC1) |
| 3 | DINB (converter IC2) |
| 4 | SCLK (common) |
| 5 | GND |
| 6 | VCC |
| | |
| Analog Interface – J2 | |
| 1 | VOUTA (converter IC1) |
| 2 | N/C |
| 3 | VOUTB (converter IC2) |
| 4 | N/C |
| 5 | GND |
| 6 | VCC |

The PmodDA2 is usually powered from the Digilent system board connected to it. The power and ground connections are on pins five and six of the digital interface connector J1. Alternatively, the PmodDA2 can be powered from an external power supply provided through pins five and six of the analog interface connector J2. In this case the power select jumper on the system board should be set to disconnect power from the system board to J1. Damage may result if two power supplies are connected at the same time. The Digilent convention is to provide 3.3V to power Pmod modules. The PmodDA2 can be operated at any power supply voltage between 2.7V and 5.5V, however caution should be exercised if using any voltage greater than 3.3V, as damage to the Digilent system board could result.

*1) Implementation of DAC:* As we know that DAC is used to convert the digital samples into the analog signal(sine or square or etc.).In this project we are using the 12 bit DAC means it coverts each time 12 bit value into the analog signal.

We do the modulation by taking from the message signal from the ADC and the carrier signal from the DDS and after the modulation or demodulation process we will place the final output value on the DAC means at the final we will get from the DAC module. It is also the 2-channel DAC means at a time we can take the two outputs and also we can give the two inputs. At last after getting the output on the DAC we will check the voltage levels by multimeter or we can see the signal on CRO and we will measure the amplitude and time period values.

*D.UART*

UART is a type of "asynchronous receiver/transmitter", a piece of computer hardware that translates data between parallel and serial interfaces. UARTs are commonly used in conjunction with other communication standards such as EIA RS-232. A UART is usually an individual (or part of an) integrated circuit used for serial communications over a computer or peripheral device serial port .

*E. Implementation of Microblaze*

In our project the Microblaze place a main important role. It is a soft core processor. And we know about the two type processors, those are Micrblaze and the Power Pc. The main difference between the microblaze and power pc is, microblaze is a soft core processor and the power pc is a hard core processor.

*1) Microblaze:* Which is a soft core processor, the some part of the fpga will acts as a microblaze processor by implementing the hardware description language means by the vhdl code we are making act of some part of fpga as microblaze. So it is called as soft core processor. No need of any external hardware circuitry.
Modulation techniques are selected in the synthesized unit. It consists of 4 types of modulation techniques.

## III. MODULATION TECHNIQUES

In this project we are implementing Microblaze soft core processor. And this processor will take the information from the Pc by using UART. So from that, we receive the commands in HEXA, ASCII format. By using these commands only we can change our parameters of modulation techniques like setting frequency, setting azimuth angle, changing work mode, self testing and output RF signal. This function we will implementing by coding. According to these commands the modulation techniques are select in the synthesized unit. Those modulation techniques are described below.

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*A. Amplitude Modulation*

It is the process where, the amplitude of the carrier is varied proportional to that of the message signal. Amplitude Modulation with carrier Let m(t) be the base-band signal, m(t) ←→ M(ω) and c(t) be the carrier, c(t) = Ac cos(ωct). fc is chosen such that fc >> W, where W is the maximum frequency component of m(t).

The amplitude modulated signal is given by

$s(t) = Ac [1 + kam(t)] \cos(\omega ct)$
$S(\omega) = \pi Ac/ 2 (\delta(\omega - \omega c) + \delta(\omega + \omega c)) + kaAc /2 (M(\omega - \omega c) + M(\omega + \omega c))$

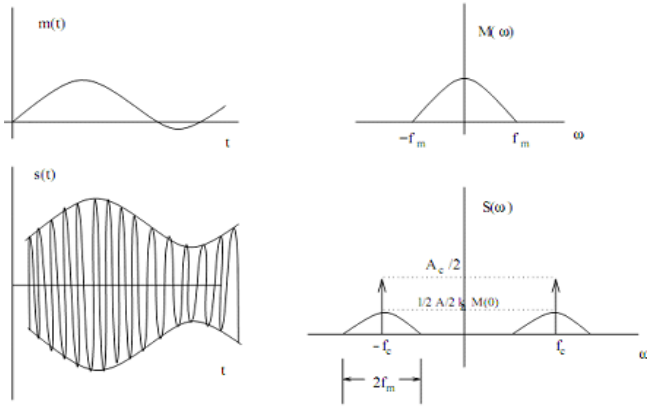


**Figure 5. Amplitude modulation**

Figure 5 shows the spectrum of the Amplitude Modulated signal.

- ka is a constant called amplitude sensitivity. kam(t) < 1 and it indicates percentage modulation.
- Modulation in AM: A product modulator is used for generating the modulated signal as shown in Figure 6.

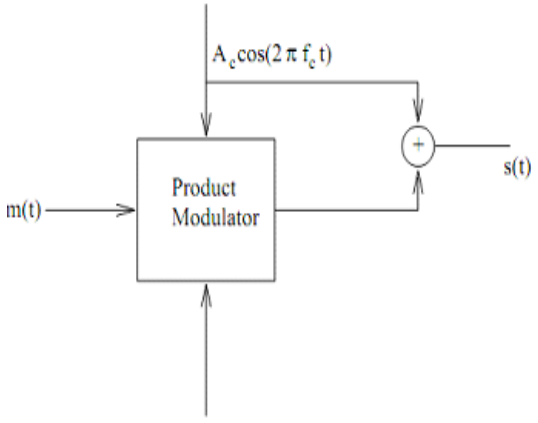


**Figure 6. Modulation using product modulator**

*1) Double Side Band - Suppressed Carrier (DSB-SC) Modulation:* In AM modulation, transmission of carrier consumes lot of power. Since, only the side bands contain the information about the message, carrier is suppressed. This results in a DSB-SC wave. A DSB-SC wave s(t) is given by

$s(t) = m(t)Ac \cos(\omega ct)$
$S(\omega) = \pi Ac/ 2 (M(\omega - \omega c) + M(\omega + \omega c))$

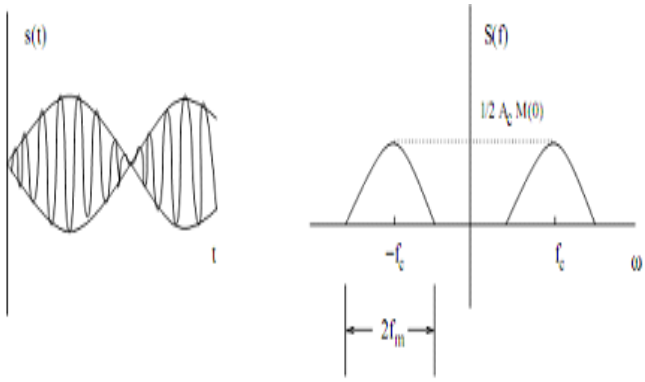


**Figure 7. DSB-SC modulation**

• *Modulation in DSB-SC:* Here also product modulator is used as shown in Figure 6, but the carrier is not added. Figure 7 shows the spectrum of the DSB-SC signal.

*B. Frequency Modulation*

This chapter will introduce the reader to the second analog form of modulation. This type of modulation scheme is known as angle modulation. Angle modulation can be further subdivided into two distinct types: frequency modulation (FM) and phase modulation (PM).

The classic definition of FM is that the instantaneous output frequency of a transmitter is varied in accordance with the modulating signal. Recall that we can write an equation for a sine wave as follows:

E ( t) = E sin( t + f)

While amplitude modulation is achieved by varying E , frequency modulation is realized by varying in accordance with the modulating signal or message. Notice that one can also vary f to obtain another form of angle modulation known as phase modulation (PM). Later we will examine the relationship between FM and PM. See Figure 3.4 for a time display of a typical FM signal.

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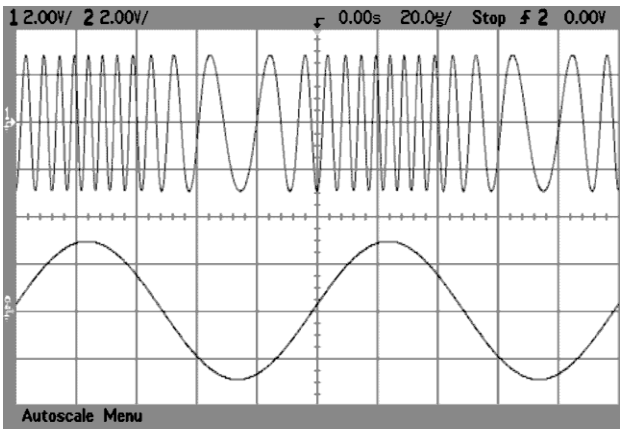


**Figure 8. A typical FM signal shown with the modulating signal**

An important concept in the understanding of FM is that of frequency deviation. The amount of frequency deviation a signal experiences is measure of the change in transmitter output frequency from the rest frequency of the transmitter. The rest frequency of a transmitter is defined as the output frequency with no modulating signal applied.

*C. Binary Phase Shift Keying*

Like any form of shift keying, there are defined states or points that are used for signaling the data bits. The basic form of binary phase shift keying is known as Binary Phase Shift Keying (BPSK) or it is occasionally called Phase Reversal Keying (PRK). A digital signal alternating between +1 and -1 (or 1 and 0) will create phase reversals, i.e. 180 degree phase shifts as the data shifts state.

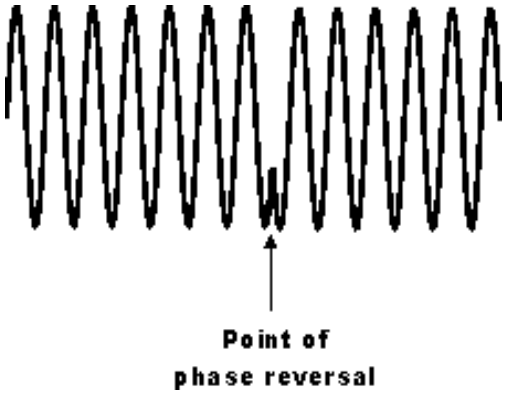


**Figure 9. Binary phase shift keying, BPSK**

*D. Quadrature Phase Shift Keying (QPSK)*

The QPSK modulator can modulate two signals in same frequency band. Each signal is to be converted from analog to digital, then modulate one signal with sine and another with cosine which gives four different phase shifts with two signals, by adding these two phase shifted signals we get QPSK output signal.

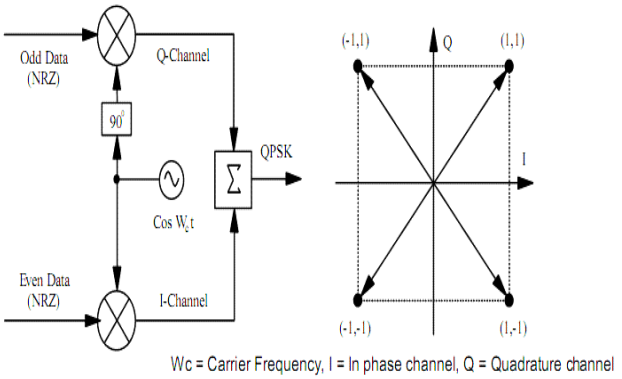


**Figure 10. Quadrature Phase Shift Keying**

- Quadrature Phase Shift Keying is effectively two independent BPSK systems (I and Q), and therefore exhibits the same performance but twice the bandwidth efficiency.
- Quadrature Phase Shift Keying can be filtered using raised cosine filters to achieve excellent out of band suppression.
- Large envelope variations occur during phase transitions, thus requiring linear amplification.

If we observe the QPSK output waveform, we found that there is a sinusoidal wave shifting with the change in symbol and the phase angle is same for different symbols. It means the output waveform will be the same sinusoidal signal with starting from since it is only the sinusoidal signal. We just have to start the output signal from different phase angle according to input symbol (00, 01, 11, 10). The phase shift angle may be 0°, 90°, 180° and 270° or it may be 45°, 135°, 225° and 315°.

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## IV. SIMULATION RESULTS

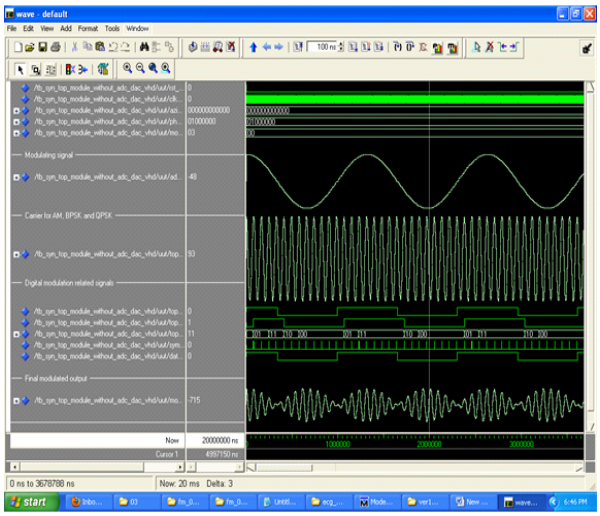

**Figure 11. Simulation of DSB-SC**

The above figure shows the simulation diagram of DSB-SC. The message signal is stored in the buffer. Carrier signal is generated through DDS IP Core. When the mod-command word is 00 then we will get the final output as AM modulated waveform.

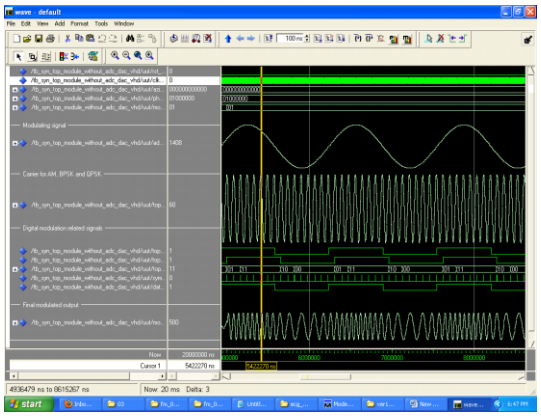

**Figure 12. Simulation of FM**

The above figure shows the simulation diagram of FM. The message signal is stored in the buffer. For FM DDS signal is acts as message signal. Carrier is generated through code. When the mod-command word is 01 then we get the FM as final output.

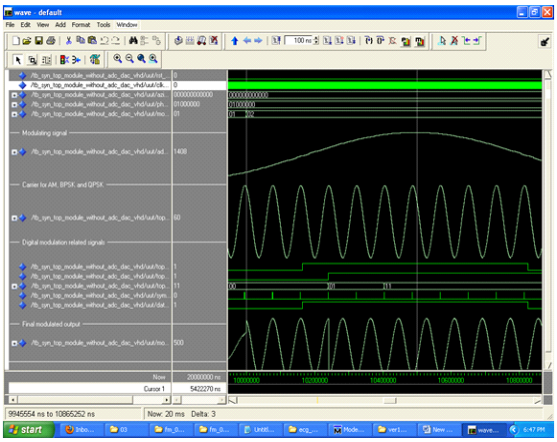

**Figure 13. Simulation of BPSK**

The above figure shows the simulation diagram of BPSK. Message signal is stored in buffer. Carrier is generated through IP Core. When the mod- command word is 02 we will get the BPSK as final output. In BPSK the phase is shifted for 0, 1, then we will get the bit reversal.

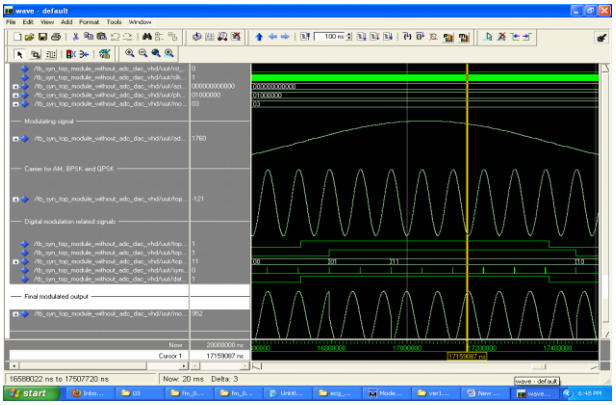

**Figure 14. Simulation of QPSK**

The above figure shows the simulation diagram of QPSK. When the mod-command word is 03 then we will get the QPSK as final output. Output signal form different phase angle according to input symbol (00, 01, 11, 10). The phase shift angle may be 0°, 90°, 180° and 270° or it may be 45°, 135°, 225° and 315°.

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## V. CONCLUSION

In this paper, the digital signal generator of radio navigation is implemented by soft processor microblaze whose key portion is achieved in a single FPGA chip, which overcomes the disadvantage of low accuracy and flat tuning in trditional method. The analog and digital modulation techniques AM, FM, BPSK, and QPSK have been done. Through the numerical test and simulation results, the veracity and precision is confirmed. The microblaze program results are captured on Spartan 3E FPGA. Favourable result has been acquired in practical application .

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