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Wide Band Rate Conversion Using CIC Filters for Wireless Communication Receivers

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***Abstract*— Cascaded integrator comb (CIC) filters are widely used in multi-rate digital signal processing for both the decimation and interpolation. Digital down converter is plays important role in wireless communication system. In this paper we can design FPGA based optimized decimation filters for wireless communication receivers. Digital down converter(DDC) utilizes the major resources and cost efficient. In DDC we can design DDS to generate the arbitrary wave forms. However the proposed filters is designed to decimate the signal high sample rate to low sample rate. The decimation filter converts the sampling rate 50 MHz to 6.25 MHz by the decimation fctor 8. In the DDC we can implement CFIR and PFIR for efficient result. This architecture will be implemented in VHDL and tested in Xilinx FPGAs. Modelsim is used for simulation and Xilinx ise is used for synthesis report. The design methodology is implemented on Spartan 3E FPGA based xc5vlx110t-3-ff1136 target device. On chip verification can be done on chipscope.**

***Keywords*—CFIR, CIC, DDC, Decimator, FPGA.**

I. INTRODUCTION

Nowadays digital electronics are plays major role due to wide usage digital representation of wireless communication for transmit and reception. In digital signal processing, a digital down-converter (DDC) converts a digitized real signal centered at an intermediate frequency (IF) to a baseband complex signal centered at zero frequency. In addition to down conversion, DDC's typically to implement the decimator and interpolator.

A DDC consists of three basic components they are direct digital synthesizer (DDS), a low pass filter (LPF) and a down sampler. Digital Down-Converter (DDC) is a major component of digital radios[9]. The DDC consists of a Numeric Controlled Oscillator (NCO) and a mixer to down convert the input signal to baseband. In the DDC interpolator and decimator are used to up conversion and down conversion in multi rate digital signal processors. In decimation process CIC filters are anti aliasing filters before down sampling. In this project we can design decimation filter for convert the signal high sampling rate to low sampling rate.

The DDC will be uses the lower resource utilization ,low power consumption, high speed and low circuit complexity in wireless communication systems to reduce the cost of main design. FPGAs are re configurable and it has better speed and provide flexibility ,high speed and better performance[2]. FPGA not only increase the speed and but also improve the overall performance of the design.

A fundamental part of many communications systems is Digital down Conversion (DDC). Digital radio receivers often have fast ADC converters delivering vast amounts of data; but in many cases, the signal of interest represents a small proportion of that bandwidth. A DDC allows the rest of that data to be discarded, allowing more intensive processing to be performed on the signal of interest. As an example, consider a radio signal lying in the range 39-40MHz. The signal bandwidth is 1MHz. However, it is often digitized with a sampling rate over 100MHZ, representing in the region of 200Mbyte/second. The DDC allows us to select the 39-40MHz band, and to shift its frequency down to baseband. Once this is complete, the sampling rate can be reduced with a 1MHz bandwidth, a sampling rate of 2.5MHz would be fine - giving a data rate of only 5Mbyte/second. The Figure 1. Shows functionality of DDC.

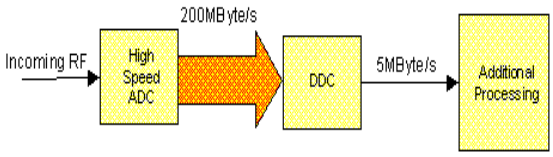

Fig.1. An overview of DDC function.

Any suitable low-pass filter can be used including FIR, IIR and CIC filters. The most common choice is a FIR filter for low amounts of decimation (less than ten) or a CIC filter followed by a FIR filter for larger down sampling ratios. DDC's are most commonly implemented in logic in field-programmable gate arrays or application-specific integrated circuits.

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While software implementations are also possible, operations in the DDS, multipliers and input stages of the low pass filters all run at the sampling rate of the input data. This data is commonly taken directly from analog to digital converters (ADC's) sampling at tens or hundreds of MHz, which is beyond the real time computational capabilities of software processors.

II. Cascaded Integrator Comb (CIC) Filters

Cascaded integrator-comb (CIC), or Hogenauer filters are proposed by Eugene B. Hogenauer[3]. CIC filters are multirate filters used for realizing large sample rate changes in digital systems. These are multiplier-less structures, consisting of only adders, subtractors and registers (delay elements). Therefore, CIC filters are more efficient than conventional FIR filters , especially in fixed-point applications. The CIC filter consists equal number of integrator sections and comb sections. The integrator section operating at high sampling rate and comb section operates at low sampling rate. In the recent years various techniques are proposed by researchers[4] - [10]. In the DDC the decimation filter can be done poly phase and CIC based DDC can be implemented in wireless communication systems. In this paper author presents an optimized design of Non-Recursive CIC filter structure[12].

CIC decimation filter: Eugene B. Hogenauer invented the CIC filter structures is economical class of linear phase, FIR filter. It do not require multipliers and uses less amount storage to store the filter coefficients. It has the two basic building blocks of a CIC filters are integrator and comb. Integrator is running at high sampling rate.

It is a ingle pole IIR filter with unity feedback coefficient.

$$y(n)=y(n-1)+x(n) \qquad (1)$$

The transfer function of the integrator in the z-plane is given by

$$H_1(Z) = \frac{1}{1-z^{-1}} \qquad (2)$$

The power response of integrator is -20 db per decade but infinite gain at DC due to the single pole at Z = 1. In this integrator output is high sampling rate. Integrator section has a delayed input and output and it has feedback. This project contains 8- stage of integrators. The basic integrator shown in below figure.2.

In the CIC filters comb section running at low sampling rate. In this sampling rate is high when integrator output. The high sampling rate is converted by decimation filter given as the input to the comb filter. The basic comb filter is shown in below fig.3.

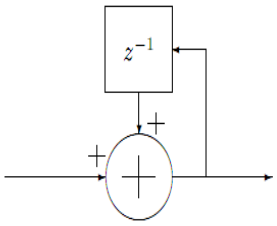

Fig.2. Basic Integrator

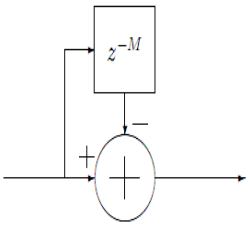

Fig.3.Basic Comb

A comb filter running at the low sampling rate, f_s / R, for the rate of change of R in odd symmetric FIR filter described by

$$y(n)=x(n)-x(n-RM) \qquad (3)$$

In this equation,

M - design parameter or differential delay.

M can be any positive integer, but it is usually limited to 1 or 2. The corresponding transfer function at is given by

$$H_C(z)=1-z^{-RM} \qquad (4)$$

When R = 1 and M = 1, the power response of comb high pass function 20 db per decade. The .when the CIC filter designed equal number of integrator sections and equal number of comb sections i.e N number integrators and N number comb filters. The transfer function of a filter given by

$$H(Z)=H_I^N(Z)H_C^N(Z) = \frac{(1-Z^{-RM})}{(1-Z^{-1})^N} \qquad (5)$$

The structure of CIC decimation filter is shown in Fig. 4.

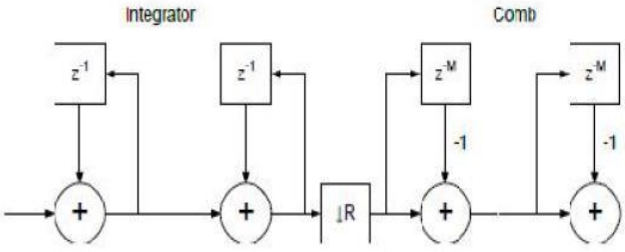

Fig.4. CIC decimation filter

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In this project we are implementing digital down converter (DDC) for FPGA based wireless communication system applications. Study and realization of CIC filters and Polyphase Filters for digital down converter. Implementation of Digital synthesis techniques and optimization on FPGA. The DDC block diagram using CIC Filters is shown in the below fig.5.

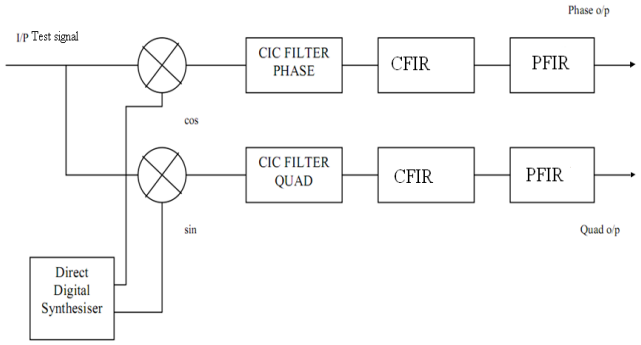

Fig.5. CIC based DDC block diagram

Digital Down-Converter (DDC) is a key component of digital radios. The DDC performs the frequency translation necessary to convert the high input sample rates found in a digital radio, down to lower sample rates for further and easier processing. The DDC consists of a Numeric Controlled Oscillator (NCO) and a mixer to down convert the input signal to baseband. The baseband signal is then low pass filtered by a Cascaded Integrator-Comb (CIC) filter followed by two FIR decimating filters to achieve a low sample-rate. In this CFIR filter is used to compensate passband droop, PFIR is used to provide additional filtering.

III. Proposed Methodology

In the DDC based CIC filters The Test signal is generated by mixing the two signals with frequencies of 300 kHz and 2 MHz. These two signals are generated by using two DDS cores as shown in the below figure 6.

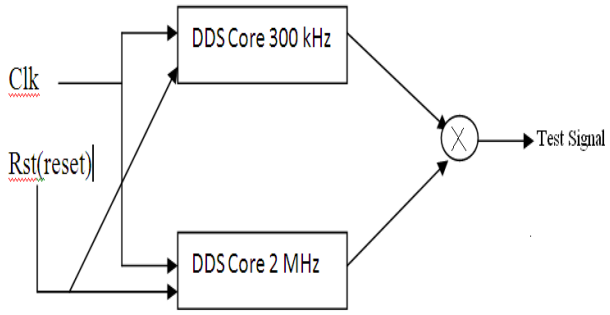

Fig.6. Test signal generator using two DDS cores

Direct Digital Synthesizer (DDS) or (NCO-Numerically Controlled Oscillator) is used to generate the cos and sin signals. These two signals are mixed and given as the input to the CIC Filter In Phase and Quad Phase sections separately. The output of the CIC Filter is followed by the CFIR (Compensating FIR Filter) and PFIR (Programmable FIR Filter).

The CFIR Filter is used to compensate the output of the CIC Filter and PFIR Filter is used to solve the bandwidth issues in both the sections.

The CIC filter frequency response does not have a wide, flat pass band. To overcome the magnitude droop, a FIR filter that has a magnitude response that is the inverse of the CIC filter can be applied to achieve frequency response correction. Such filters are called "compensation filters." The cic filter response shown below fig.7. the CIC filters exhibits the passband droop.CFIR filter is used compensate this pass band droop.

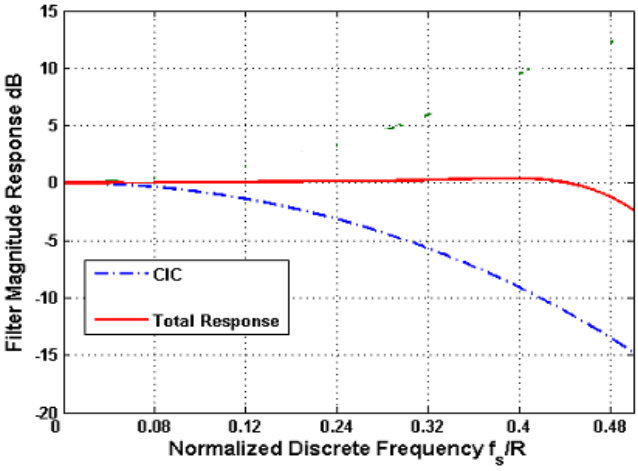

Fig.7. CIC filter Response

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CFIR filter is used compensate this pass band droop. Compensating FIR filter is required to compensation the magnitude response non-linearity in pass band. Compensation filter response shown in below fig.8.

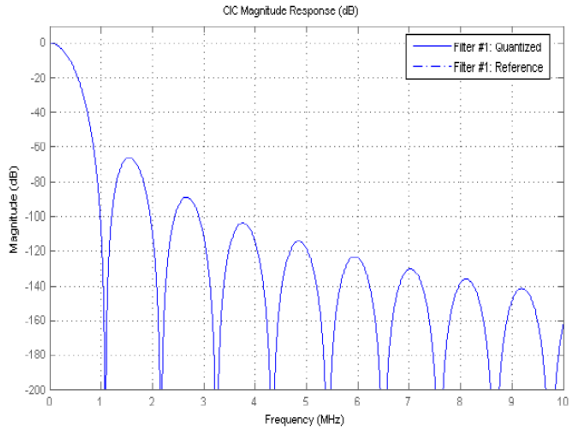

Fig.8. compensation filters response

For data rate down conversion, the compensation filter follows the CIC filter. the compensation FIR filter pre-conditions the data and is followed by a CIC filter.

Equation shows the magnitude response of an N-stage CIC filter at high frequency (f_S):

$$|H(f)| = \left| \frac{\sin(\pi M f)}{\sin(\frac{\pi f}{R})} \right|^N \quad \text{------- Equation(I)}$$

An example of a CIC filter magnitude response

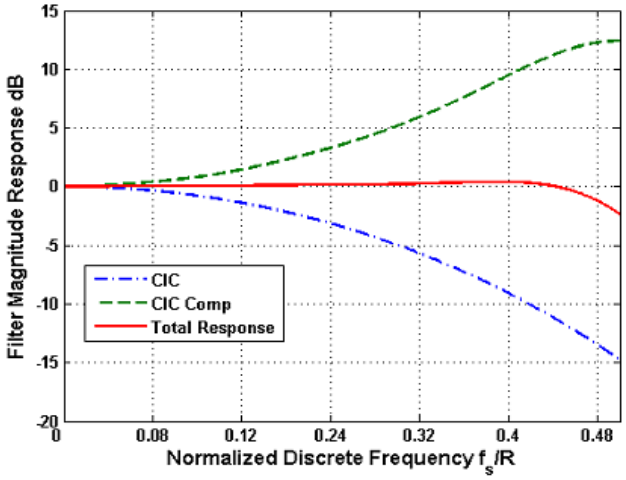

Fig.9. Response after using the CFIR Filter

To achieve a flat pass band, the compensation FIR filter should have a magnitude response that is the inverse of above Equation. The response after using the CFIR Filter is as shown in the above figure.9.

IV. Simulation Results

The proposed design shown in below figure is implemented on Spartan 3E FPGA device using Modelsim Xilinx ISE simulator.

The system is designed with decimation factor 8 and it is implemented in 3 stages. The input signal is 50 MHz is became after down sampling 6.25 MHz. the single stage implementation of purposed filter is shown in below figure.

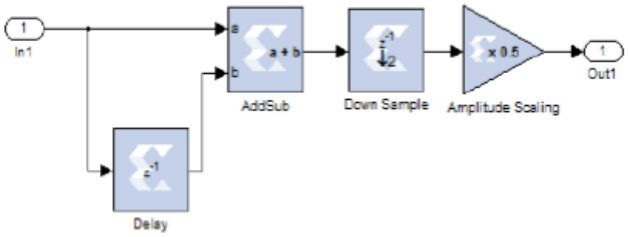

Fig.10. Single stage implementation of purposed filter

There is a practial problem in implementing it. If the input signal has any small DC value then it simply accumulates over time and goes to either maximum or minimum value of the 2s complement number. Hence the gain of feedback term is reduced in the integrator equation to realize a stable filter. The equation y[n]= 0.5y[n-1] + x[n] is implemented. In this case the output will be stable.

The following Fig.8. and Fig.9. show the simulation results obtained for CIC based DDC. Detailed labels are written above each waveform.

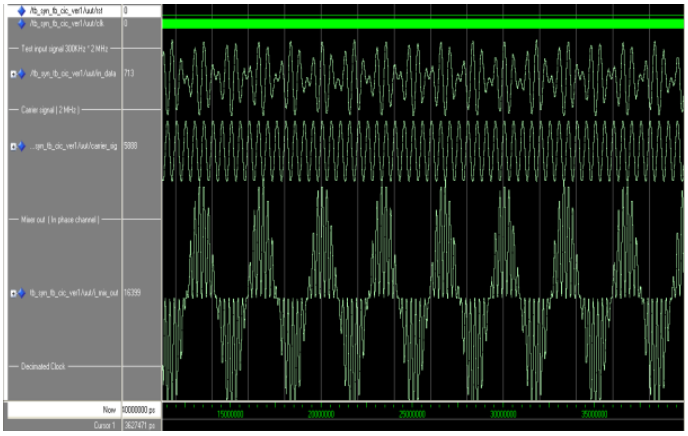

Fig.11. Mixer output

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The test input signal is a mixed signal with 300KHz and 2 MHz. This signal is obtained by multiplying two DDS's outputs. This is the first waveform (after rst and clk signals) in the above figure. The second waveform is 2 MHz carrier which is generated with another DDS. Fig.8. is mixer output for in phase (I) channel.

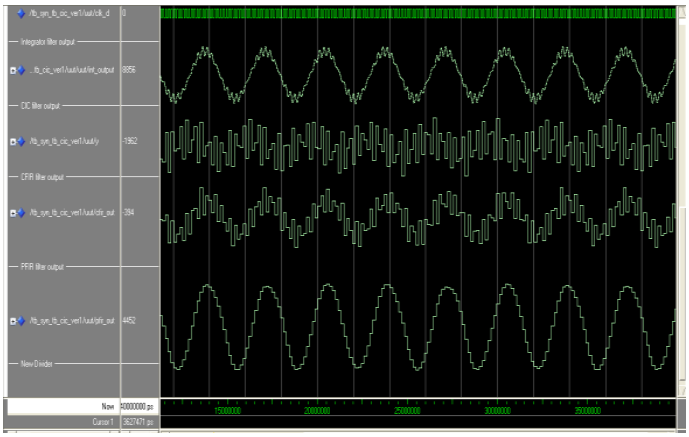

Fig.12. CIC output

In these simulation results the first decimated clock is shown. This is decimated with a factor of 8. The second fig.9. and above fig.8. is the integrator stage output of CIC architecture. The next waveform is the complete CIC output. We can notice the CIC output is coming with decimated clock. In the CIC output we can get some noise because all the signals are mixed in that signal. We can get the CIC output by connecting CFIR to CIC filter. The PFIR filter is used to select the required frequency from signal.

Table I
Synthesis of CIC based DDC

Device utilization summary:		
Selected Device : 3s500efg320-4		
Number of IOs : 50		
1	Number of Slices: 3519 out of 4656	75%
2	Number of Slice Flip Flops : 2908 out of 9312	31%
3	Number of 4 input LUTs : 5040 out of 9312	54%
4	Number of bonded IOBs : 26 out of 232	11%
5	Number of MULT18X18SIOs : 9 out of 20	45%
6	Number of GCLKs : 3 out of 24	12%
7	Number of DCMs : 1 out of 4	25%

V. CHIPSCOPE RESULTS

The CIC after porting on FPGA is tested with chipscope. Because of memory limitations on FPGA each stage output is not capture on chipscope. Only the input and output are connected to chipscope data port. The below figure shows the test input signal for DDC which is 300KHz mixed with 2 MHz carrier. It can be see that the output is 300 KHz sin wave.

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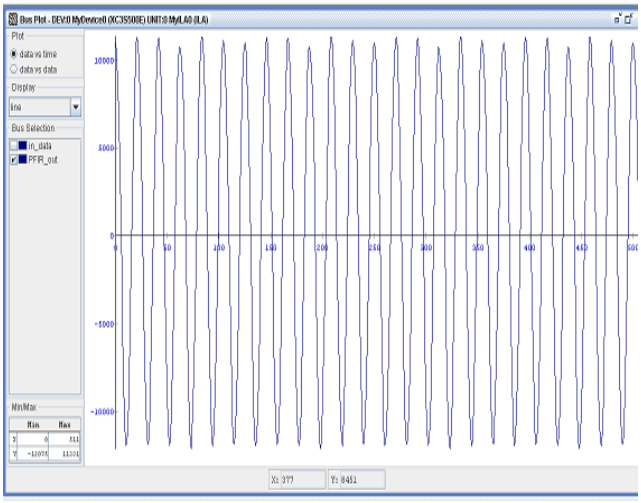

Fig.13. PFIR output on Spatarn 3E FPGA

VI. CONCLUSION

The issues in designing digital down converter are studied. The main applications where DDC becomes the front end of software defined radio are understood. Two architectures; CIC based and polyphase based are analyzed and implemented for FPGAs. VHDL generic coding style is followed to make the blocks highly configurable so that the same design with generic map can be configured for different decimation rates. Stability issues in realizing CIC filters are studied. CIC filter followed by compensating FIR filter are realized to achieve flat magnitude response over pass band. The programmable filter after CFIR is realized to further rejected aliased band due to decimation. FDA tool is used for generating the filter coefficients for various filters. The inverse SINC function is taken for realizing CFIR filter. Filter coefficients are converted to fixed point and used in VHDL coding. Polyphase based DDC is also realized with generic coding style. Decimation is achieved with Xilinx digital clock manager (DCM) component. Simulation and chipscope results are verified for both architectures. The chipscope results are captured at 50 MHz clock speed on Spartan 3E FPGA.

The comparison shows polyphase takes more area in comparison with CIC based filter. Timing results show that both work at high frequency.

REFERENCES

[1] S. K. Mitra, "Digital Signal Processing—A Computer Based Approach", Second Edition, McGraw-Hill, 2001.

[2] Patrick Longa and Ali Miri "Area-Efficient FIR Filter Design on FPGAs using Distributed Arithmetic", IEEE International Symposium on Signal Processing and Information Technology, Vol. 4, pp.248-252, 2006.

[3] E. B. Hogenauer, "An economical class of digital filters for decimation and interpolation", IEEE Transactions on Acoustics, Speech and Signal Processing, Vol. 29, No. 2, pp. 155–162, 1981.

[4] H. Aboushady, Y. Dumonteix, M. M. Louerat and H. Mehrez, "Efficient polyphase decomposition of comb decimation filters in Sigma-Delta analog-to-digital converters", IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, Vol. 48, No. 10, pp. 898 – 903, 2001.

[5] Gordana Jovanovic Dolecek and Sanjit K. Mitra,"A New Two-Stage CIC-Based Decimation Filter",Proceedings of the 5th International Symposium on image and Signal Processing and Analysis , pp. 218 – 223, 2007.

[6] Gordana Jovanovic-Dolecek and Sanjit K Mitra, "On Design of CIC Decimation Filter with Improved Response", IEEE 3rd International Symposium on Communications, Control and Signal Processing, pp. 1072 - 1076, 2008.

[7] D.J. Allred, H. Yoo, V. Krishnan, W. Huang, and D. Anderson, "A Novel High Performance Distributed Arithmetic Adaptive Filter Implementation on an FPGA", in Proc. IEEE Int. Conference on Acoustics, Speech, and Signal Processing (ICASSP'04), Vol. 5, pp. 161-164, 2004.

[8] Ricardo A. Losada and Richard Lyons,"Reducing CIC Filter Complexity",IEEE Signal Processing magazine, pp.124-126,July 2006.

[9] F.J.A. de Aquino, C.A.F. da Rocha, and L.S. Resende, "Design of CIC filters for software radio system", IEEE International Conference on Acoustics, Speech, Signal Processing, pp. III-225-228, May 2006.

[10] R. Uusikartano and J. Takala, "Power-efficient CIC decimator architecture for fs/4-downconverting digital receivers", IEEE International Midwest Symposium on Circuits and Systems, Vol. 3, pp. 1315 – 1318, Dec. 2004.

[11] M Madheswaran and V Jayaprakasan "Implementation and comparison of different CIC filter structure for decimation", ICTACT journal on communication technology, Vol: 04, Issue: 02, pp. 709-716, June 2013.

[12] V Elamaran, R Vaishnavi, A Maxel Rozario, Slitta Maria Joseph and Aylwin Cherian, "CIC for decimation and interpolation using Xilinx System Generator", IEEE International conference on Communication and Signal Processing, pp. 622-626, April 2013.

[13] Matthew P. Donadio, "CIC Filter Introduction", IEEE International Symposium on Communications , pp. 1-6, July 2000.

[14] Ramesh Bhakthavatchalu, Karthika V.S., Lekshmi Ramesh and Budhota Aamani, "Design of Optimized CIC Decimator and Interpolator in FPGA", IEEE International Multi-Conference on Automation, Computing, Communication, Control and Compressed Sensing (iMac4s), pp. 812-817, 2013.

[15] Xilinx, Inc., "Virtex-V platform FPGA handbook", Vol.3, No. 1, 2012.

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