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VHDL Implementation of High Performance Digital Up-converter Using Multi-DDS Technology for Radar Transmitters

S. Mounika[1], K. Sandeep kumar[2], G. Srujan[3]

[1]*M.Tech Scholar, Aurora's Scientific Technological and Research Academy, Hyderabad, TS, India.*
[2,3]*Associate Professor, Dept of ECE. Aurora's Scientific Technological and Research Academy, Hyderabad., India*

***Abstract*— Direct Digital Synthesizer (DDS) is a type of frequency synthesizer used for creating arbitrary waveforms from a single, fixed-frequency reference clock. Radar is an object detection system which uses radio waves to determine the range, altitude, direction, or speed of objects. Digital Up-conversion is the core technology in digital radar transmitter. To achieve high sampling rate, we have to use high clock frequency hence a high hardware clock is required. In this paper we are using the Multi-DDS (10 DDS) technology which is based on parallel processing, a large bandwidth signal can be produced at conditions of a lower hardware clock. This output signal is used to generate the Radar signal with high sampling rate (50 MHz). Similarly Multi-DDS technology gives a high-efficient solution. With this by using lower hardware clock high sampling rate can be achieved. As this paper presents the results based on a system (i.e. Spatarn-3E FPGA) whose clock frequency is 50MHz.**

***Keywords*—Digital Up-conversion, Multi-DDS algorithm, Parallel processing**

I. INTROUDUCTION

Digital radar transmitters widely used because of its low development costs, flexibility and small size[1].But with the Traditional digital up conversion process is used to achieve high sampling rate, we have to use high clock frequency hence high hardware clock is required.

With this Multi-DDS (10 DDS) technology a lower hardware clock and high sampling rate can be achieved. As this paper presents the results based on a system (i.e Spatarn- 3E FPGA) whose clock frequency is 50MHz.By assuming that 1DDS will give 5MHz clock Frequency. In this paper we are using a multi-DDS technique by assuming (10 DDS) that 10 DDS are working parallel to generate 50MHz Clock .sampling Rate increases from 5MHz to 50MHz in order to meet the requirement of Radar applications.

RADAR (Acronym for Radio Detection and Ranging) is an object-detection system that uses radio waves to determine the range, altitude, direction, or speed of objects. A radar system has a transmitter that emits radio waves called radar signals in predetermined directions. When these come into contact with an object they are usually reflected or scattered in many directions.

The radar signals that are reflected back towards the transmitter are the desirable ones that make radar work.

Radar receivers are usually, but not always in the same location as the transmitter. Although the reflected radar signals captured by the receiving antenna are usually very weak, they can be strengthened by electronic amplifiers. More sophisticated methods of signal processing are also used in order to recover useful radar signals.

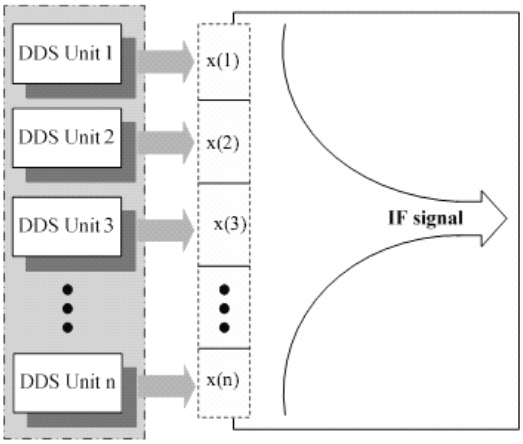

Fig 1. Block Diagram of Multi-DDS [1]

The above figure shows generic DDS which is a combination of n DDS modules. According to this paper for getting 50MHz sampling rate 10 DDS are suffice. With this we are generating the radar signal and finally got the radar signal with high sampling rate.

II. MULTI-DDS TECHNOLOGY

Direct Digital Frequency Synthesis (DDFS or simply DDS), also known as Numerically Controlled Oscillator (NCO). Direct Digital Synthesizer (DDS) is a type of frequency synthesizer used for creating arbitrary waveforms from a single, fixed-frequency reference clock. Applications of DDS include: signal generation, local oscillators in communication systems, function generators, mixers, modulators, sound synthesizers and as part of a digital phase-locked loop.

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A basic Direct Digital Synthesizer consists of a frequency reference, a numerically controlled oscillator (NCO) and a digital-to-analog converter (DAC).The reference provides a stable time base for the system and determines the frequency accuracy of the DDS. It provides the clock to the NCO which produces at its output a discrete-time, quantized version of the desired output waveform whose period is controlled by the digital word contained in the Frequency Control Register. The sampled, digital waveform is converted to an analog waveform by the DAC. The output reconstruction filter rejects the spectral replicas produced by the zero-order hold inherent in the analog conversion process.

Many possibilities for frequency generation are open to the designer, ranging from phase-locked-loop (PLL) based techniques for very high-frequency synthesis, to dynamic programming of digital-to-analog converter (DAC) outputs to generate arbitrary waveforms at lower frequencies. But the DDS technique is rapidly gaining acceptance for solving frequency (or waveform) generation requirements in both communications and industrial applications because single-chip IC devices can generate programmable analog output waveforms simply and with high resolution and accuracy.

A. Single DDS unit principle

A digitally-controlled method of generating multiple frequencies from a reference frequency source has evolved called Direct Digital Synthesis (DDS). The NCO main purpose is to generation the carrier signals (cosine).The main advantage is ROM based techniques will be used for area optimization.

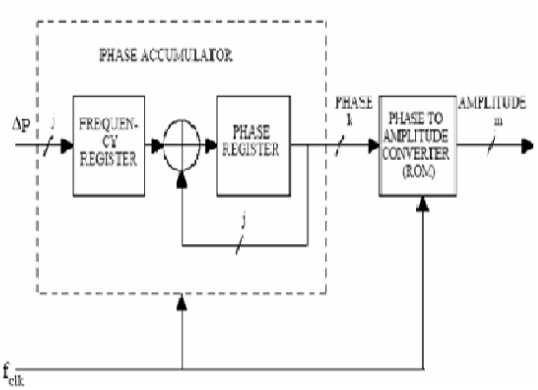

Fig 2. NCO (OSCILLATOR)

A numerically controlled oscillator (NCO) is a digital signal generator which creates a synchronous, discrete-time, discrete valued representation of a waveform. NCOs are often used in conjuction with a Digital-to-analog converter (DAC)at the output to create a direct digital synthesizer(DDS).Applications of DDS include: signal generation, local oscillators in communication systems, function generators, mixers, modulators, sound synthesizers and as part of a digital phase-locked loop.

A basic Direct Digital Synthesizer consists of a frequency reference, a numerically controlled oscillator (NCO) and a digital-to-analog converter (DAC).

The reference provides a stable time base for the system and determines the frequency accuracy of the DDS. It provides the clock to the NCO which produces at its output a discrete-time, quantized version of the desired output waveform (often a sinusoid) whose period is controlled by the digital word contained in the Frequency Control Register. The sampled, digital waveform is converted to an analog waveform by the DAC. The output reconstruction filter rejects the spectral replicas produced by the zero-order hold inherent in the analog conversion process.

Phase Accumulator (PA):

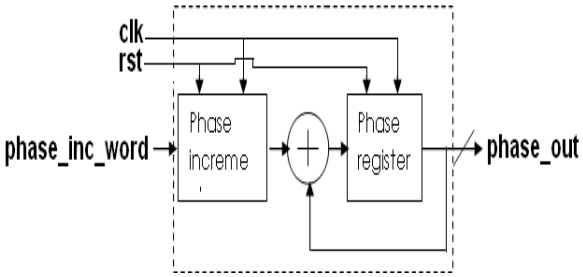

Fig 3. Phase Accumulator

Which adds to the value held at its output a frequency control value at each clock sample. The phase accumulator consists of phase increment register, adder and phase register. The phase increment register stores the instantaneous phase increment values resulting from frequency modulation control block. Look up Tables are programmed to consider 255 as highest phase value and phase increment by one results next cycle of waveform.

All the blocks are connected with common clock and reset signals. The delta phase value decides the phase increment for each clock pulse. Hence decides the resulting signal frequency. The Frequency modulating instantaneous value is added to the delta phase value which causes instantaneous change in frequency. Due to the digital nature of the modulator only at each clock tick the modulating signal value shall affect the resulting frequency. If the modulating signal is analog then an Analog to Digital converter must be used to digitize the modulating signal which can be used in NCO. The phase accumulator produces accumulated phase value for each clock pulse. In case if the DDS is used for phase modulation then instantaneous phase modulating signal value is added to the phase output of phase accumulator.

The Parallel in Parallel Out shift register cells are required in phase accumulator block to hold frequency and phase values. Synchronization is required between the phase increment register and phase register. This is achieved by connecting a common clock signal.

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Generic is used in VHDL implementation which allows to instantiate the PIPO component any bit size.

The heart of the system is the phase accumulator whose content is updated once for each clock cycle. Each time the phase accumulator is updated, the digital number M stored in the delta phase register is added to the number in the phase accumulator register. The truncated output of the phase accumulator serves as the address to a sine (or cosine) lookup table. Each lookup table contains the corresponding digital amplitude information for one complete cycle of a sine wave. The lookup table therefore maps the phase information from the phase accumulator into a digital amplitude word, which in turn drives the DAC.

A Phase-to-Amplitude converter (PAC):

This uses the phase accumulator output word usually as an index waveform look-up table (LUT) to provide a corresponding amplitude sample. Sometimes interpolation is used with the look-up table to provide better accuracy and reduced phase error noise.

A binary accumulator consists of an N-bit binary adder and a register. Each clock cycle produces a N-bit output consisting of the previous output obtained from the register summed with the frequency control word(FCW) which is constant for a given output frequency. The adder is designed to overflow when the sum of the absolute value of its operands exceeds its capacity(2n-1).The overflow bits is discarded so the output word width is always equal to its input word width .The PAC can be simple read only memory containing 2M contiguous sample of the desired output waveform.

B. Multi-DDS Algorithm

Direct digital synthesizer uses a lookup table to generate sine and cosine signals. And since most of the signals can be decomposed into a number of sine and cosine signals, Seen by the sampling theorem, when system clock is CLK, the highest frequency that a DDS can generate is CLK ÷2. If the higher frequency is required with the same clock, Multi-DDS technology supports a high-efficient solution. N channel parallel DDS units work in the clock of CLK can produce a signal with the frequency of N .CLK ÷2 Hz.

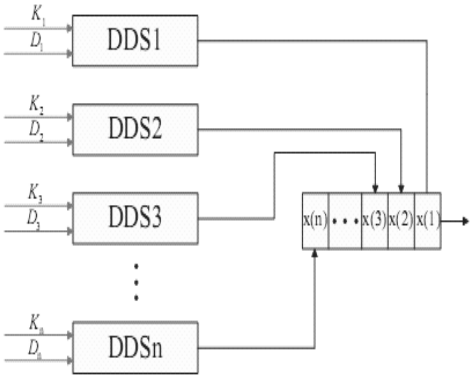

Fig 4. Structure of Multi-DDS [1]

DDS_1 to DDSn are the N channel parallel DDS units. K_i and D_i is the representative for the ith frequency control word and phase control word. Input having Ten DDs signals i.e n=10. By Assuming that 1DDS will give 5 MHz clock Frequency which is of sampling rate of 5MHz.In this paper we are using a multi-DDS technique by assuming (10 DDS) that 10 DDS are working parallel to generate 50 MHz Clock. Sampling Rate increases from 5 MHz to 50 MHz in order to meet the requirement of Radar applications.

C. Core Architecture Overview

The core consists of two main parts, a Phase Generator and SIN/COS LUT, which can be used independently or together with an optional dither generator to create a DDS capability. A time-division multi-channel capability is supported, with independently configurable phase increment and offset parameters. Below Figure 5 provides a block diagram of the DDS Compiler core.

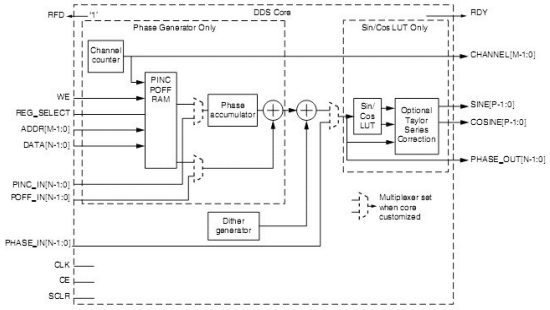

Fig 5. DDS Compiler core [1]

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Phase Generator:

The Phase Generator consists of an accumulator followed by an optional adder to provide addition of phase offset. When the core is customized the phase increment and offset can be independently configured to be either fixed, programmable or supplied by the PINC_IN and POFF_IN input ports respectively.

When set to programmable, registers are implemented with a bus interface, consisting of ADDR, REG_SELECT, WE, and DATA signals. The address input, ADDR, specifies the channel for which DATA is to be written when multi-channel, with REG_SELECT specifying whether DATA is phase increment or offset.

When set to fix the DDS output frequency is set when the core is customized and cannot be adjusted once the core is embedded in a design.

SIN/COS LUT:

When configured as a SIN/COS LUT, the Phase Generator is not implemented, and the phase is input via the PHASE_IN port, and transformed into the sine and cosine outputs using a look-up table. Efficient memory usage is achieved using half wave and quarter wave storage schemes. The presence of both outputs and their negation are configurable when the core is customized. Precision can be increased using optional Taylor Series Correction. This exploits Xtreme DSP slices on FPGA families that support them to achieve high SFDR with high speed operation.

Phase Generator and SIN/COS LUT (DDS):

The Phase Generator is used in conjunction with the SIN/COS LUT to provide either a Phase Truncated DDS or Taylor Series Corrected DDS. An optional dither generator can be added between the two blocks to provide a Phase Dithered DDS.

TABLE I.
Device Utilization Summery

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Total Number Slice Registers	1,085	9,312	11%	
Number used as Flip Flops	1,084			
Number used as Latches	1			
Number of 4 input LUTs	750	9,312	8%	
Number of occupied Slices	796	4,656	17%	
Number of Slices containing only related logic	796	796	100%	
Number of Slices containing unrelated logic	0	796	0%	
Total Number of 4 input LUTs	906	9,312	9%	
Number used as logic	639			
Number used as a route-thru	156			
Number used as Shift registers	111			
Number of bonded IOBs	14	232	6%	
IOB Flip Flops	12			
Number of RAMB16s	17	20	85%	
Number of BUFGMUXs	3	24	12%	
Number of BSCANs	1	1	100%	
Number of RPM macros	12			
Average Fanout of Non-Clock Nets	2.31			

III. RADAR SYSTEMS

The term "RADAR" is generally understood to mean a method by means of which short electromagnetic waves are used to detect distant objects and determine their location and movement. The term RADAR is an acronym from Radio Detection and Ranging.

A complete Radar measuring system is comprised of a Transmitter with antenna, a Transmission path, the Reflecting Target, a further Transmission path (usually identical with the first one), and a Receiver with antenna. Two separate Antennas may be used, but often just one is used for both Transmitting and Receiving the Radar signal.

A Radar Pulse Train is a type of Amplitude Modulation of the Radar Frequency Carrier wave, similar to how Carrier waves are modulated in Communication Systems. In this case, the information signal is quite simple: a single Pulse Repeated at Regular intervals. The common Radar Carrier Modulation, known as the Pulse Train is shown below. The common parameters of Radar as defined by referring to Figure 6.

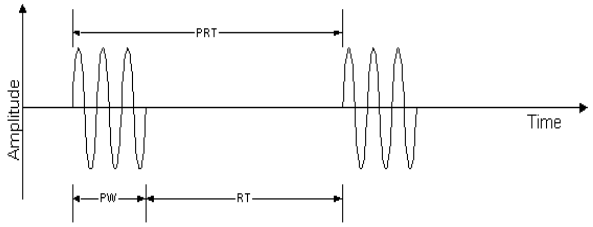

Fig 6. Pulse Train

PW = Pulse Width. PW has units of Time and is commonly expressed in ms. PW is the duration of the Pulse. RT = Rest Time. RT is the Interval between pulses. It is measured in ms. PRT = Pulse Repetition Time. PRT has units of Time and is commonly expressed in ms. PRT is the interval between the start of one pulse and the start of another. PRT is also equal to the Sum, PRT = PW+RT. PRF = pulse repetition frequency. PRF has units of time^{-1} and is commonly expressed in Hz (1 Hz = 1/s) or as Pulses per Second (PPS). PRF is the number of pulses transmitted per second and is equal to the inverse of PRT. RF = Radio Frequency. RF has units of time^{-1} or Hz and is commonly expressed in GHz or MHz. RF is the frequency of the Carrier wave which is being modulated to form the Pulse Train.

Radar (Radio Detection and Ranging):

The Radar dish or antenna transmits pulses of Radio waves or Microwaves that bounce off any object in their path. The object returns a tiny part of the wave's energy to a dish or Antenna that is usually located at the same site as the Transmitter.

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The Radar was invented in the early 1900's but it took 30 years of development to make it useful in reality. The breakthrough came with the Second World War, where a lot of energy and resources were spent on the development of Radar. The electronic principle on which Radar operates is very similar to the principle of sound-wave reflection. If you shout in the direction of a sound-reflecting object (like a rocky canyon or cave), you will hear an echo. If you know the speed of sound in Air, you can then estimate the distance and general direction of the Object. The time required for an echo to return can be roughly converted to distance if the speed of sound is known. Radar uses electromagnetic energy pulses in much the same way, as shown in Figure 6. The Radio-Frequency (RF) energy is transmitted to and Reflected from the Reflecting Object. A small portion of the Reflected energy returns to the Radar set. This returned energy is called an ECHO, just as it is in sound terminology. Radar sets use the echo to determine the direction and distance of the Reflecting object.

It refers to electronic equipment that detects the presence of Objects by using reflected electromagnetic energy. Under some conditions a Radar system can measure the direction, height, distance, course and speed of these objects. The frequency of electromagnetic energy used for Radar is unaffected by darkness and also penetrates fog and clouds. This permits radar systems to determine the position of Airplanes, Ships, or Other Obstacles that are invisible to the naked eye because of Distance, Darkness, or Weather. Modern Radar can extract widely more information from a Target's ECHO signal than its Range. But the calculating of the range by measuring the delay time is one of its most important functions.

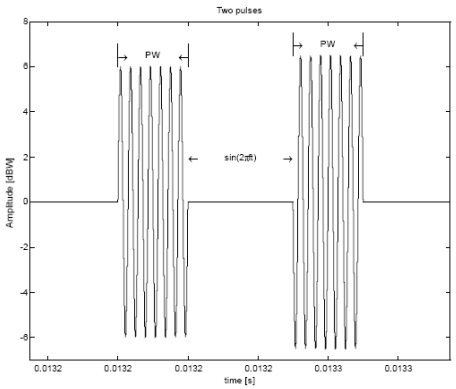

Fig7. The plot above shows two pulses where the carrier Frequency is the frequency in the sine wave.

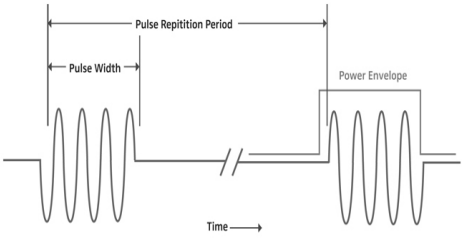

Fig 8.Radar signal

IV. MULTI-DDS OUTPUT INTERFACED TO RADAR

In this paper we are generating the radar signal and applying the Multi–DDS output to this Radar Signal and got the Radar Signal with high Sampling Rate.

This Process includes the radar signal it contain Pulse Width and Pulse Repeteition period. Pulse Repetetion period wait for the signal which is bombarded and wait for echo. Previously we have normal resources by which we having a low sampling rate. For Radar efficiency we need a high sampling rate. With this Multi-DDS (10 DDS) technique we are sending high sampling rate signal. In the duration of Pulse Width time it sends the signal while in the duration of Pulse Repetition time it observes the echo signal. By this Way it continuously observes for detection of objects etc.

V. RESULTS AND ANALYSIS

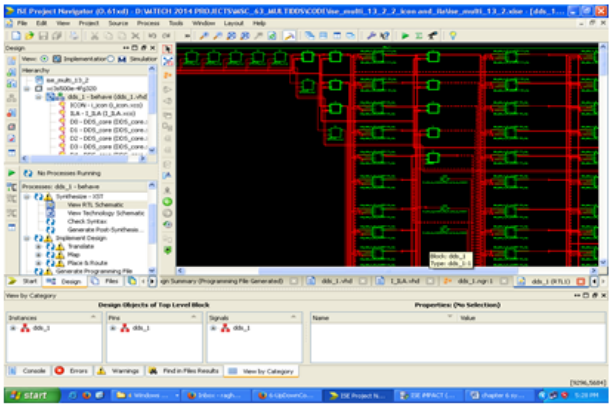

Fig 9.RTL Schematic of Multi-DDS (10 DDS)

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Simulation Result

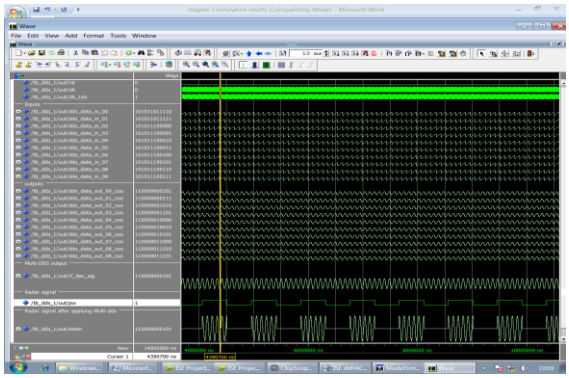

Fig 10. Simulation Outputs of Multi-DDS (10 DDS)

Fig.10 shows simulation results of Reset, Clk and Clk_10x then DDs input having Ten DDs signals. Afterwards the analog waveform shows the output of each DDS. RF_DAC_SIGNAL is the final output of Multi-DDs having high Sampling Rate. With extension to this we are generating the radar signal and applying the multi –DDs output to this Radar Signal and got the Radar Signal with high Sampling Rate.

Chipscope Result

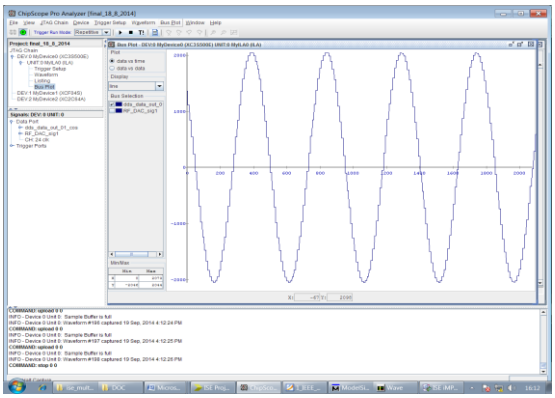

Fig 11. Chipscope result at 50MHz clock speed on Spatarn 3E- FPGA

VI. CONCLUSION

In this paper the proposed Multi-DDS (10 DDS) algorithm can be used to achieve a sampling rate of 50 MHz by using lower hardware clock of 5 MHz. This solution eliminates the need of large Hardware clock. We Developed an algorithm for synthesizable Multi-DDS (10 DDS) unit in HDL (Hardware Description Language) using Xilinx ISE 13.2 and Modelsim Xilinx Edition (MXE) 6.6b. Simulation, Synthesis and Chipscope results are verified for Multi-DDS (10 DDS). The Chipscope results are captured at 50 MHz clock speed on Spartan-3E FPGA.

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About the authors:

S. Mounika received B.Tech Degree in ECE from JNTUH, Telangana in 2012, Pursuing M.Tech in the stream of VLSI System Design at Aurora's Scientific, Technological and Research Academy,(Affiliated to JNTU) Hyderabad, Telangana.

K. Sandeep Kumar, Associate Prof, ECE Dept, Aurora's Scientific, Technological and Research Academy, Hyderabad, Telangana. B.Tech in ECE from Sri Sai Institute of Technology and Science, Rayachoty, A.P, in 2006. M.Tech in VLSI System Design from Aurora's Scientific, Technological and Research Academy, Hyderabad, Telangana, in 2012. Area of interest VLSI Signal processing, Low Power VLSI Design.

G. Srujan, Associate prof, ECE Dept, Aurora's Scientific, Technological and Research Academy, Hyderabad, Telangana.
B.E in ECE from Karnatak University, Dharwad, in 2001.
M.Tech in VLSI Design from Bharath University, Chennai in 2005.