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A Comparative Study of Linearization Techniques of CMOS LNA

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***Abstract*—this paper presents a comparative study of few linearization techniques of LNA for system like GPS which requires a highly linear LNA. The topology is analysed in terms of noise performance, gain, linearity and impedance matching.**

***Keywords*—Cascode amplifiers, inductive source degeneration, Negative Feedback,Derivative superposition, Modified DS method, Post-linearization technique.**

I. INTRODUCTION

During the last few years, there has been an intense interest on the design of the GPS system due to its many applicable properties like these days it find its way into cars, planes, boats, construction equipment ,farm machinery and many more. GPS is defined as Global Positing System which is a worldwide radio navigation system formed from a constellation of 24 satellites and their ground stations. Since in many countries, it is compulsory to have GPS services in the cellular communication. This facilitate the user to have same services at a time, that's it can simultaneously receive and process GPS information while still activating the function of the cellular communication.

But to enable this functionality few changes is required in the low noise amplifier (LNA) of a RF circuit design to improve the RF performance of the front-end circuitry. LNA is the first block of a RF receiver [1] and the LNA design should be such that it much provide minimum noise figure (NF) and large gain, low power consumption and producing stable 50 ohm input impedance with sufficient linearity to suppress interference and maintain high sensitivity. This can be achieved by improving the input third-order intercept point (IIP3) of the LNA. Also input 1-dB compression point (IPIdB) and the isolation from the cellular power amplifier to the GPS LNA input must be increased. But the linearization techniques must be simple and should not compromise with the noise figure and the gain. Therefore linearization of LNA becomes a challenging factor in the LNA design, often requiring innovative techniques.

Different proposals can be found in the literature to efficiently solve the challenging problem of linearity of the LNA. In this paper some linearity approaches are reviewed.

II. LNA ARCHITECTURES

In the designing of low noise amplifiers, there are some important goals. To achieve these goals different LNA architectures are available. In this section, some of the LNA architectures are discussed.

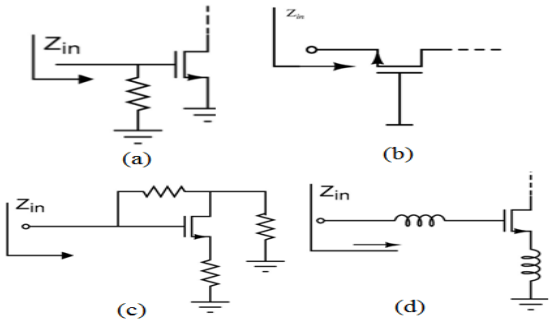

Fig.1. Common LNA Architectures (a) Resistive Termination (b) 1/gmTermination (c) Shunt-Series Feedback (d) Inductive Degeneration

Four common LNA architectures are shown in the fig.1 resistive matching is the most straightforward approach to achieve the broadband 50 matching at the input. However, the resistor adds its thermal noise to the circuit whileattenuates the incoming signal by a factor of two before it reaches the gate of the transistor. These two effects make an unacceptably high noise figure of the circuit and therefore it is not practical in many applications of LNA. Common-gate configuration or $1/g_m$ Termination is another method for realizing a resistive input matching in which a common-gate transistor is made to match the impedance by choosing $g_m$equal to $1/R_s$. But due to lower gm, a MOSFET transistor requires a high current for Rs = 50Ω which in turn result in high power consumption. Another drawback of common-gate matching topology is that when source resistance is known, it will have constant g_m.

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Unlike the resistive termination matching, a Shunt-Series Feedback does not attenuate the signal by a noisy resistance before hitting the gate of the amplifying device and hence the noise figure is expected to be much lower. But the feedback resistor continues to generate thermal noise of its own which relatively increases the noise figure. Therefore this architecture is not applicable for LNA. The fourth architecture that is the inductive degeneration employs inductive source. Inductive source degeneration matching topology provides a perfect match without adding any noise to the system (resistive matching) or giving any restrictions on the device g_m (common-gate matching).It also has the advantage ofhigh gain, because of all this feature it is widely architecture in LNA design.

III. Inductive Source Degenerated LNA

A. Impedance Matching

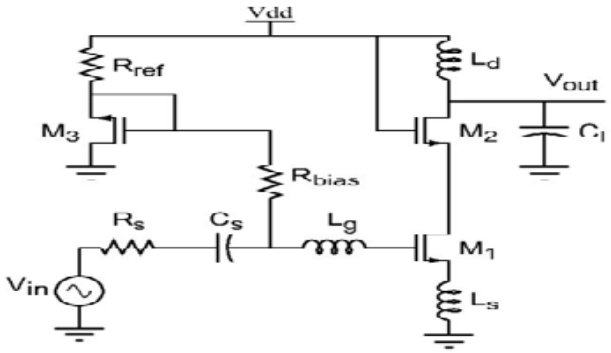

Fig.2. Cascode Inductive Degenerated LNA

A cascode inductive degenerated LNA is shown in the figure … .from the figure input impedanceZ_{in} can be calculated as

$$Z_{in}=\frac{1}{j\omega C_{gs}}+ j\omega(L_g + L_s) + \frac{g_m L_s}{C_{gs}} \qquad (1)$$

Where L_g and L_s are gate inductor and source inductor respectively.$C_{gs}$is the gate-source capacitance and $g_m$is the device transconductance.A stable 50Ω input impedance dependence on g_m can be achieved through constant g_m biasing.

B. Noise figure

Noise figure can be defined as the noise performance of a device at some particular frequency.

If a number of components are connected in cascade configuration than the equivalent noise figure of the chain will be

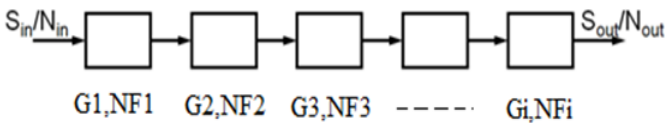

Fig.3. NF of Cascaded Stages

Therefore the total noise figure of the cascaded stage is given by

$$\mathrm{NF_{total}}=\mathrm{NF_1}+\frac{\mathrm{NF_2}-1}{\mathrm{G_1}}+\ldots\ldots\ \frac{\mathrm{NF_i}-1}{\mathrm{G_1G_2..G_{i-1}}} \qquad (2)$$

Where$\mathrm{NF_1}$is the noise figure of the first stage of the cascade stage, $\mathrm{G_1}$ is the gain of the first stage. From the equation above we can say that over noise figure of a cascade stage is dominated by $\mathrm{NF_1}$

C. Linearity

An important measure of linearity in LNA designis the input third order intermodulation point (IIP3) of thecircuit [2].and the IIP3 of the circuit shown in the fig…is given as

$$\text{IIP3 (dBm)} = IIP3_{in}\text{(dBm)} - 20log_{10}\left(\frac{1}{\omega_0 C_{gs} R_s}\right) \qquad (3)$$

Where $IIP3_{in}$ arises from the short channel CMOS transistors that exhibit velocity saturation, which gradually linearizes the ideal quadratic of the long channel drain current equation and $20log_{10}\left(\frac{1}{\omega_0 C_{gs} R_s}\right)$is due to the extra voltage that boost across the C_{gs} due to the series tank.

IV. LNA Linearization Methods

The choice of linearity methods of low noise amplifier largely depends on many parameters such as efficiency, high gain, and low noise figure [16]. Also depend on the most appropriate trade−off between competing characteristics to optimize receiver sensitivity and selectivity, and maintaining information integrity.

A. Linearization Techniques

Simple way to improve the linearity of an amplifier is to increase the bias levels which will reduces signal's input level to the amplifier. A weakly nonlinear amplifier with input X and output Y can be approximated by the first three power series terms [3] and is given by

$$Y = g_1 X + g_2 X^2 + g_3 X^3 \qquad (4)$$

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Where$g_{1,2,3}$ are the linear gain and the second/third-order nonlinearity coefficients of the amplifier respectively. The goal of linearization is to make $g_{2,3}$ small enough to be negligible, keeping only the linear termg_1, making it $Y \simeq g_1 X$. LNA nonlinearity originates from nonlinear transconductance which converts linear input voltage to nonlinear output drain current [15]. The main advantages of this method are its simplicity and speed.

B. Negative Feedback

The most popular technique to obtain high linearity is through the use of negative feedback. The traditional inductive source degenerated common-source LNA, falls under the category of feedback linearization in which the source degeneration inductor acts as the feedback circuit[15]. Though this LNA has been proven to give the best gain and noise performance for a given power, but it suffers from poor linearity due to the second order non-linearity feedback effect. Therefore this technique is not much favourable for LNA at RF frequencies due to stability reasons.

C. Optimum Biasing

Third Order Input Intercept Point is a point at which the power in the third-order product and the fundamental tone intersect, when the amplifier is assumed to be linear[15]. IIP3 is a very useful parameter to predict low-level intermodulation effects and is given by

$$IIP3 = \sqrt{\frac{4}{3}\frac{g_1}{g_3}} \qquad (5)$$

It can be seen that in the region of moderate inversion, in-between weak inversion and strong inversion, the third order derivative $g_3$becomes zero over a narrow region [4]. As shown in equation (5), it can be seen that IIP3 approaches infinity as becomes zero.

Thus any transistor biased at this point can achieve high linearity. But the problem with this mechanism is that the region over which this linearity boost can be obtained is very narrow and due to process variations this bias point is bound to change leading to a very sensitive and limited improvement.

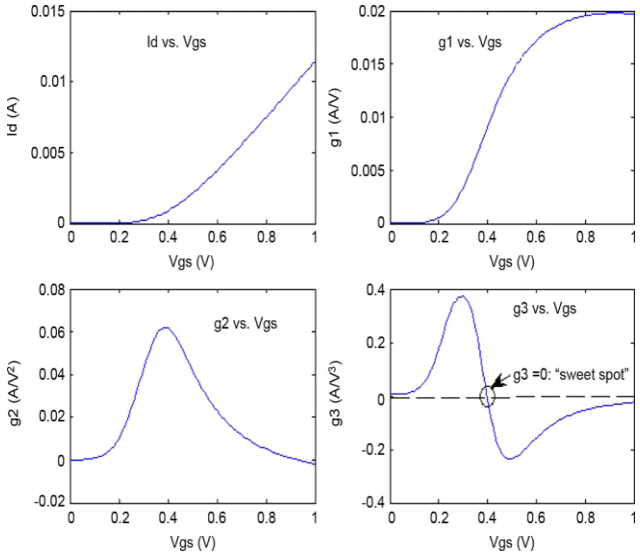

Fig.4. comparison of $I_d g_1, g_2$ andg_3 versus V_{gs} for constant V_{ds}.

Above fig 4 showsg_1,g_2 andg_3 versus V_{gs} for constant V_{ds}.We selected the gate bias V_{gs}=04V forcomparison because at this point the transconductancenonlinearity is large with sufficient gain

D. Feed-forward Technique

The feed-forward technique is also widely used to achieve linearity in an LNA. In this technique, scaled versions of the input signal are fed to two different amplifiers whose outputs are added to obtain the final output. The input signals are scaled such that the third order distortion is eliminated at the final output. This feed-forward technique is used to achieve high linearity. But this technique has several disadvantages. The gain of the amplifier is reduced at the expense of canceling the third order distortion. Due to the reduced gain, the noise figure (NF) worsens. Another disadvantage of this technique is its high degree of matching required between the circuit elements in both amplitude and phase [15]. Further, more noise is added due to more active components in the circuit. This technique is highly sensitive to mismatch between the main and auxiliary gain stages and errors in the signal scaling factor.

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This configuration also consumes more power due to two amplifier stages being used. Due to its many disadvantages, a new method called derivative superposition (DS) method is developed [5], which falls under the category of feed forward, uses two transistors connected in parallel and biased in weak and strong inversions, respectively.

E. Derivative Superposition

A different approach to feedforward technique which uses the FET transfer characteristics to obtain high linearity is the "Derivative Superposition (DS) Method". The technique allows the designs of amplifier with very low 3rd order intermodulation distortion. It also tackles the distortion reduction inside the amplifier which leads to broadband distortion reduction.

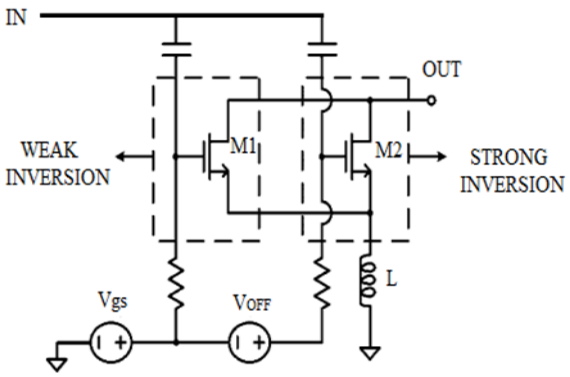

Fig. 5. Derivative Superposition method

Fig.5 shows a derivative superposition which was proposed to improve the small signal linearity performance of amplifiers. Here M1 is biased in the strong inversion region and M2 in the subthreshold region. From this we can defined he first, second and third transconductance as first, second and third derivative of the drain current w.r.t gate-source voltage as

$$g_{m1}(V_{gs}) = \frac{\partial i_{ds}}{\partial V_{gs}}\Big|_{V_{gs}} \quad (6)$$

$$g_{m2}(V_{gs}) = \frac{\partial i^2{}_{ds}}{\partial V^2{}_{gs}}\Big|_{V_{gs}} \quad (7)$$

$$g_{m3}(V_{gs}) = \frac{\partial i^3{}_{ds}}{\partial V^3{}_{gs}}\Big|_{V_{gs}} \quad (8)$$

This method addresses the problem of narrow range of values associated with optimum biasing technique for achieving high IIP3 and the problem of gain reduction associated with the feedforward technique.

The third order distortion component (g_{m3}) changes from positive to negative as V_{gs} is varied from weak inversion tostrong inversion [16]. Thus if the output currents of two transistors are added with the bias points chosen at the positive and negative peaks of and the widths scaled such that the positive and negative peaks are equal in magnitude, the output current would result in zero and thus high linearity over a wide range of bias values[6].

The drawback with DS-method is that it is valid only at very low frequencies at which the effect of circuit reactance is negligible. At high frequencies the source degeneration inductance creates a feedback path for the drain current to the gate source voltage of auxiliary transistor through the gate-source capacitance (C_{gs})[15].

F. Modified DS Method

Another method to solve the problem faced by the DS is modified DS method which addresses the issue of feedback of second order frequency components. In this method, the magnitude and phase of second order non-linearity contribution to IMD3 is tuned to cancel the third order non-linearity contribution to IMD3 thus resulting in an output current with zero IM3 component [7]. The transistor M1 is biased in strong inversion region with negative while M2 is biased in weak inversion with positive. The two source degeneration inductors L1 and L2 connected to the sources of the two transistors are used to tune the magnitude and phase of the IM3 components in each branch.

There are primarily two disadvantages involved in any of these methods using the feedforward technique involving two or more transistors connected in parallel with one or more transistors operating in weak inversion region. The first and the most important problem is that the additional weak inversion transistors added to achieve linearity degrades the noise performance of an LNA [15]. The other problem with this circuit configuration is that the weak inversion transistor loads the input node and adds extra capacitance thus affecting the input match and maximum frequency of operation. The increased capacitance would demand a larger source inductor to achieve 50Ω input matching.

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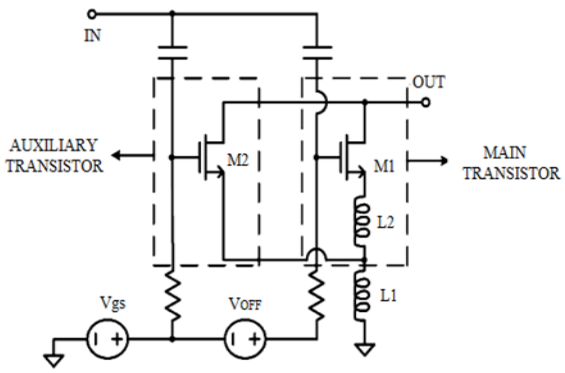

Fig.6. Modified Derivative Superposition method

G. Post-linearization Technique

To eliminate this drawback, the folded cascode PMOS topology has been proposed [8]. Moreover, this topology has the advantages of low transconductance and low current consumption. Another linearization method, post-linearization technique, is introduced. This linearization technique uses a diode connected NMOS transistor to apply to a cascodecommon gate (CG) LNA[9][15], and the linearity performance looks good.

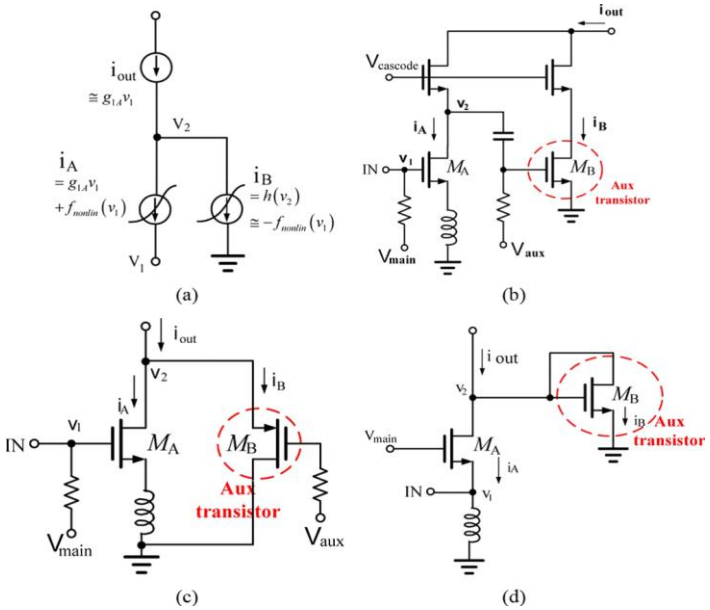

Fig ….post-distortion (a) Conceptual view, (b) circuit implementation in [10] (c) circuit implementation in [8] (d) circuit implementation in [9]

However, by applying this technique to a cascode CS LNA, the linearity improvement is needed at the penalty of degrading the gain, NF and current consumption.

TABLE I
COMPARISON OFVARIOUS LINEARITY TECHNIQUES

PAPERS	TECH (μm)	SUPPLY VOLTAGE(V)	FREQ (Hz)	S11 (dB)	S21 (dB)	S22 (dB)	NF (dB)	IIP3 (dBm)	Pdc (mw)
[11]	.18	1.8	3	-	6.5	-	1.9	15	8.9
[12]	.18	1.8	5.5		12.5		3.7	-0.45	14.4
[13]	.25	1.8	.8		14		3	3.5	15.8
[14]	.18	5.5	1.8	-12	10	-12	3.05	8.33	10.8

V. CONCLUSION

This paper compares the various linearity techniques of a low noise amplifier design which will be required in high linearity system like GPS system. From the analysis we can conclude that Post-linearization technique with inductive source degeneration topology is the best option for getting a highly linear LNA for 3-6GHZ operating frequency.

LNA design employing inductive source degeneration topology provide good matching and high gain as compared to other topology.

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