International Journal of Recent Development in Engineering and Technology
Website: www.ijrdet.com (ISSN 2347-6435(Online) Volume 3, Issue 1, July 2014)

Implementation and Comparative analysis of 32-bit Low Power Adiabatic & Hybrid Adders

Muppavarapu Sai Sumanth[1], Tulasi Sanath Kumar[2]

[1]*PG Student,* [2]*Asst. Professor, Department of Electronics & Communication Engineering, ASCET, Gudur, A.P, India.*

***Abstract*— This paper proposes different types of adder cells. Adder plays an important role in arithmetic operation in addition, subtraction, multiplication, division etc., so it is called as basic functional block. In this paper we performed a comparative analysis of various Low power Adiabatic & Hybrid adders. These adder cells are designed by using cadence 45nm tool and compared in prospects of power, delay and PDP.**

***Keywords*— PDP-Power-delay product, Adiabatic, Hybrid Adders, Sparse tree Adder, SERF Adder**

I. INTRODUCTION

Adder is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic unit(s), but also in other parts of the processor, where they are used to calculate addresses, table indices, and similar operations. It is used as a basic building block in each and every module. By this, as adder is basic block, different types of designs are implemented and analysis were made.

II. FULL ADDER

One-bit full adder has three one bit inputs (A, B, C) and produces two one-bit outputs i.e sum and carry. The relationship between input and output are:

Sum= A ⊕B ⊕C
Carry= A.B + C (A+B)

There are many logic styles for designing digital circuits which mainly influences the circuit performance. A gate is evaluated by three basic parameters: area, delay and power dissipation. Depending on the application, the emphasis will be on different parameters.

The delay time depends on the size and number of transistors, the parasitic capacitance including intrinsic capacitance and capacitance due to routing and the number of logic gates. The power consumption depends on the switching activity, size and number of transistors, glitch, leakage current of transistors and sub-current.

Power consumption in CMOS digital circuits is divided into three main parts as follows:

$P_{Total} = P_{Dynamic} + P_{Static} + P_{Short\text{-}circuit}$

- Due to charging and discharging Capacitances.
- Due to the current between power supply and ground during a transistor switching.
- Due to the leakage current and static current.

III. VARIOUS TYPES OF ADDERS

Here we analyzed various types of adders and they are as follows:

A. *Basic Adder [1]*

The design of basic adder consists of two XOR gates, two AND gates and one OR gate. The schematic diagram of basic adder is as shown in fig1 and its layout in fig2. Two XOR gates are used to produce **Sum** bit and the remaining two AND gates and one OR gate is used to produce **Carry** bit of given inputs. Due to high number of transistors, its power consumption is high. One of the most significant advantages of this full adder is high noise margins and thus reliable operation at low voltages.

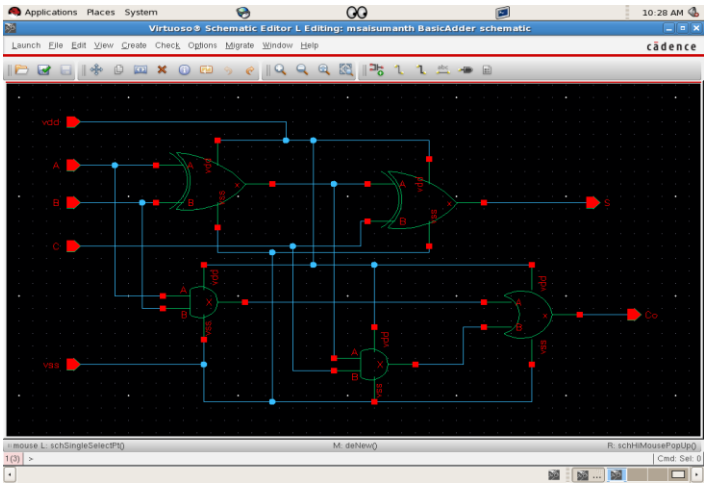

Figure 1: Schematic Of Basic Adder

International Journal of Recent Development in Engineering and Technology
Website: www.ijrdet.com (ISSN 2347-6435(Online) Volume 3, Issue 1, July 2014)

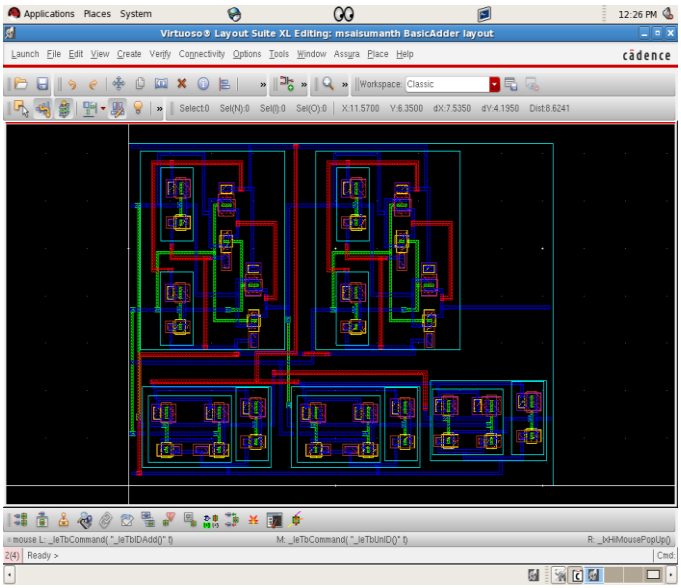

Figure 2: Layout Of Basic Adder

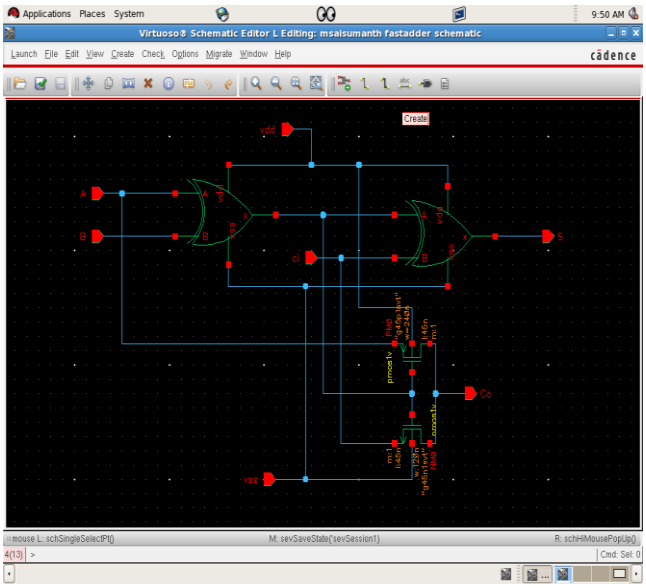

Figure 3: Schematic Of Fast Adder

B. Fast Adder

The design of fast adder consists of two XOR gates, one PMOS and one NMOS transistors. The schematic diagram of fast adder and layout are shown in fig3 and fig4. Two XOR gates are used to produce **Sum** bit and two transistors used to produce **Carry** bit by controlling them by giving A⊕B as input. Due to high number of transistors, its power consumption is high. Large PMOS transistor in pull up network result in high input capacitances, which cause high delay and dynamic power. One significant advantage of this fast adder is it produces less delay while producing carry bit at output.

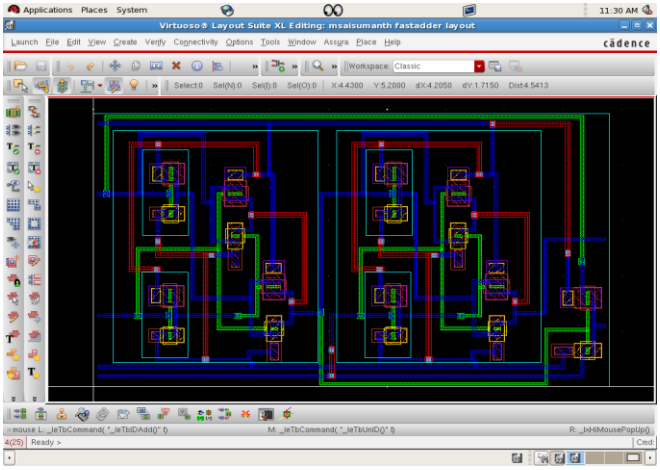

Figure 4: Layout Of Fast Adder

International Journal of Recent Development in Engineering and Technology
Website: www.ijrdet.com (ISSN 2347-6435(Online) Volume 3, Issue 1, July 2014)

C. Hybrid Adders [4], [7]

The design of hybrid adders mainly surrounds on both Pass Transistor Logic (PTL) and Gate-Diffusion Input (GDI) techniques. Here we have designed various types of hybrid adders by reducing the transistor count as follows: 22T, 17T & 14T.

22T Adder: The schematic of 22T adder and its layout are shown in fig5 and fig6. As transistor count is high power consumption is high and at the same time area is large. So transistor count is decreased to achieve low power consumption.

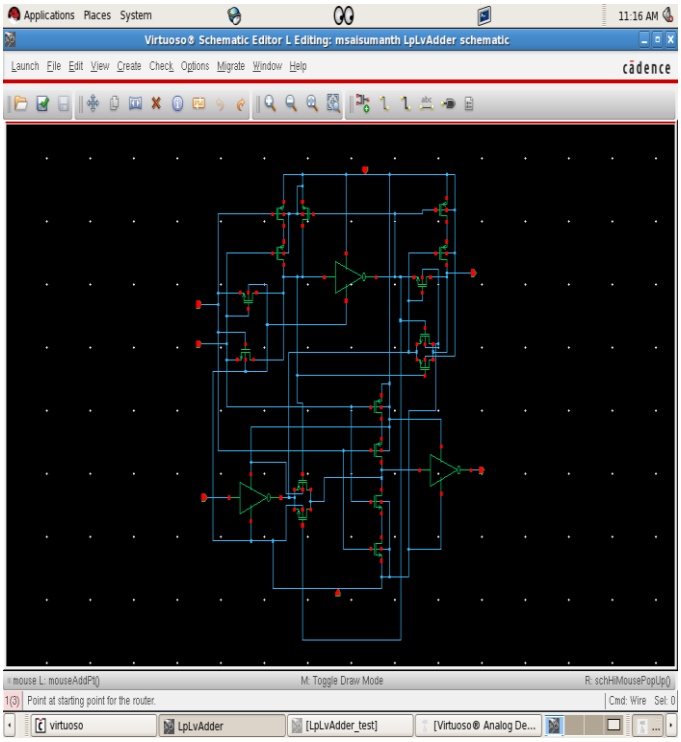

Figure 5: Schematic Of 22T Adder

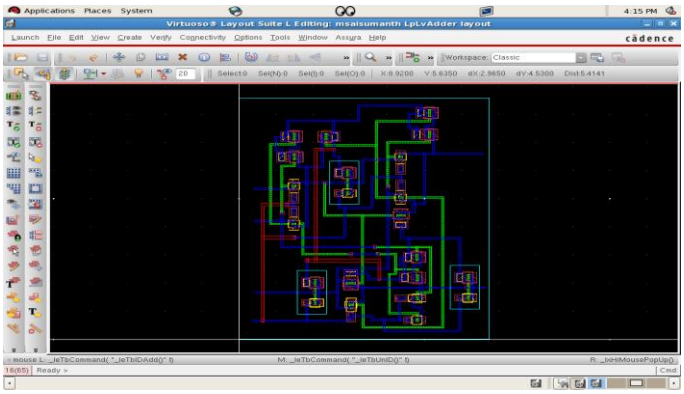

Figure 6: Layout Of 22T Adder

17T Adder: The schematic of 17T adder and its layout are shown in fig7 and fig 8.As numbers of transistors in this adder is less than 22T adder power consumption is moderate but delay is little bit high.

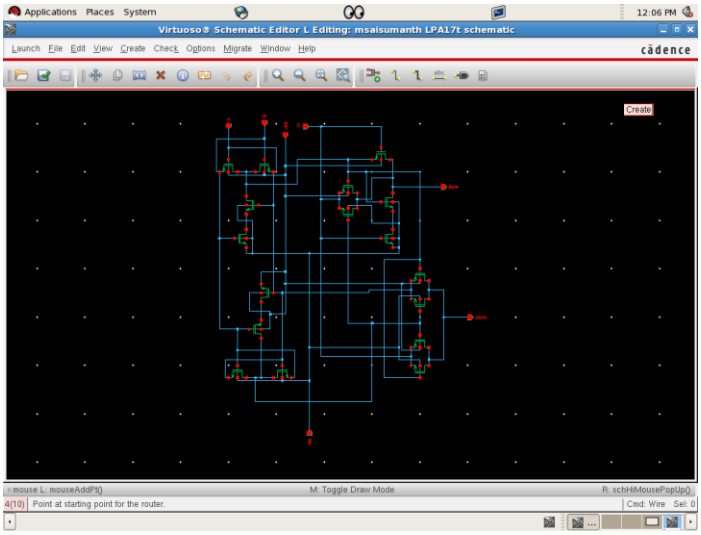

Figure 7: Schematic Of 17T Adder

International Journal of Recent Development in Engineering and Technology
Website: www.ijrdet.com (ISSN 2347-6435(Online) Volume 3, Issue 1, July 2014)

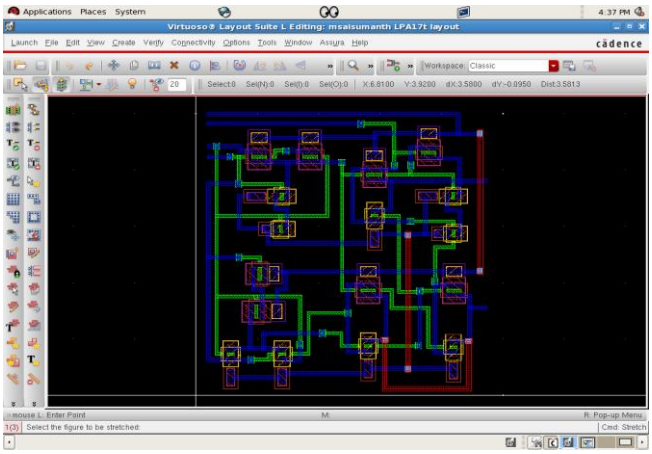

Figure 8: Layout Of 17T Adder

14T Adder: The schematic of 14T adder and its layout are shown in fig9 and fig 10.As numbers of transistors in this adder is less than 22T adder power consumption is moderate but delay is little bit high.

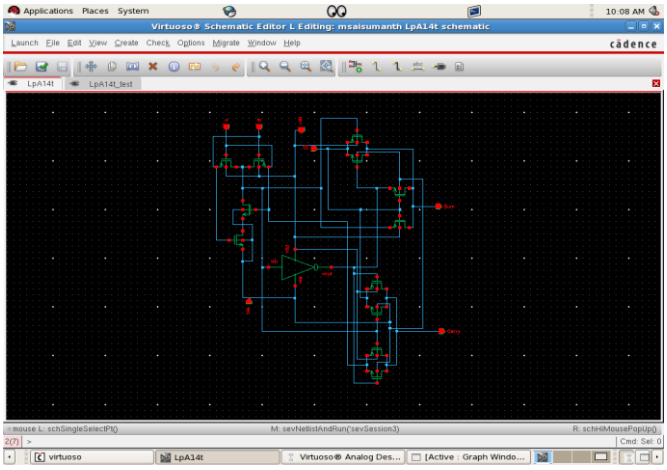

Figure 9: Schematic Of 14T Adder

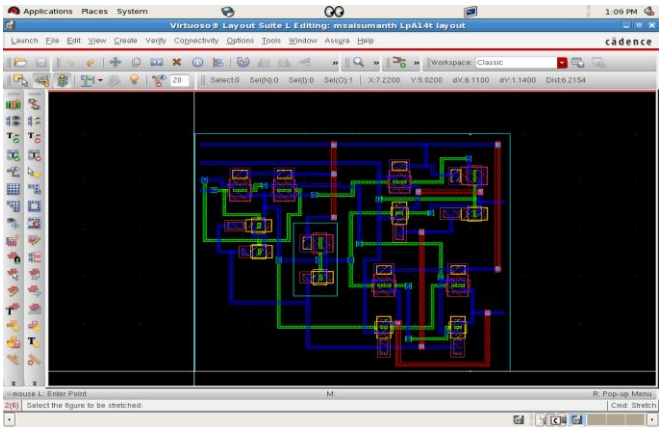

Figure 10: Layout Of 14T Adder

D. Adiabatic Adders [3], [5], [6]

Adiabatic adders are the adders which use the process of recycling. It recycles the energy instead of dissipating it directly to ground it discharges the power to supply. So in adiabatic logic power supply should be time varying signal instead of giving dc voltage. Trapezoidal signal is best to use as power clock, if it not available sinusoidal signal is also used. Here we have implemented three types of adiabatic designs.

PTAL: The schematic design of Pass transistor adiabatic logic (PTAL) and its layout are as shown in fig11 and fig12. It consists of 9 NMOS pass transistors used to produce both Sum and Carry bits as outputs. The sum and carry equations are re-arranged as follows:

Sum= (A⊕B) C' + (A⊕B)'C
Carry= (A⊕B) C + (A⊕B)'B

International Journal of Recent Development in Engineering and Technology
Website: www.ijrdet.com (ISSN 2347-6435(Online) Volume 3, Issue 1, July 2014)

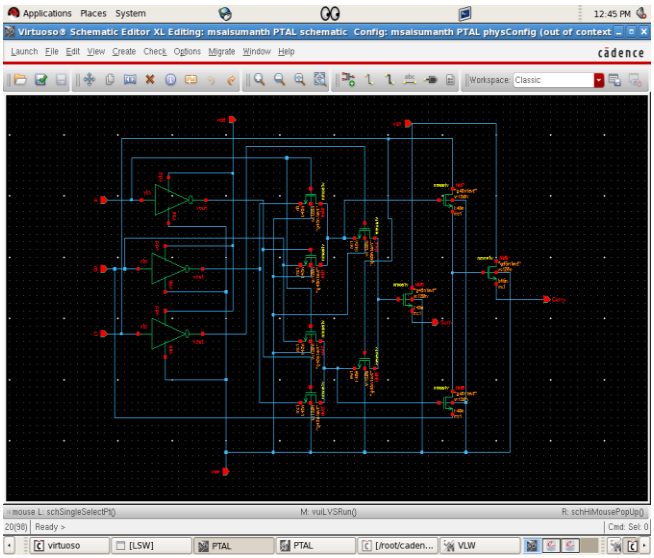

Figure 11: Schematic Of Pass Transistor Adiabatic Logic

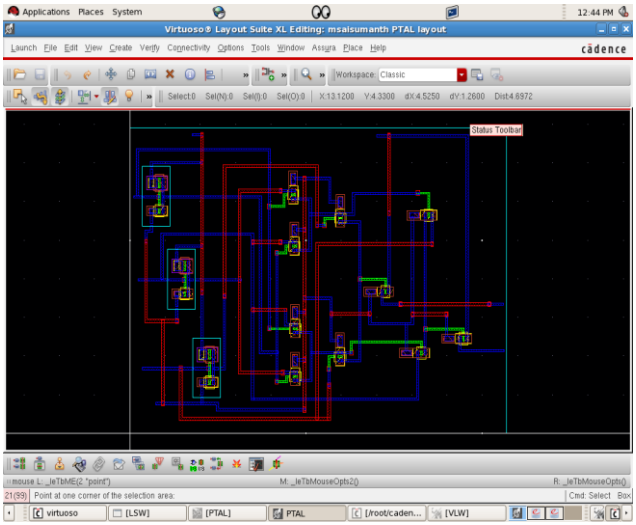

Figure 12: Layout Of Pass Transistor Adiabatic Logic

PFAL: The schematic design of Positive feedback adiabatic logic (PFAL) and its layout are shown in fig13 and fig14. The general PFAL gate consists of a two cross coupled inverters and two functional blocks F and F' (complement of F) driven by normal and complemented inputs which realizes both normal and complemented outputs. Both the functional blocks implemented with n channel MOS transistors. The equations are re-arranged as follows:

Sum=A' B' C + A' B C' + A B' C' + ABC

Carry=AB + BC + CA

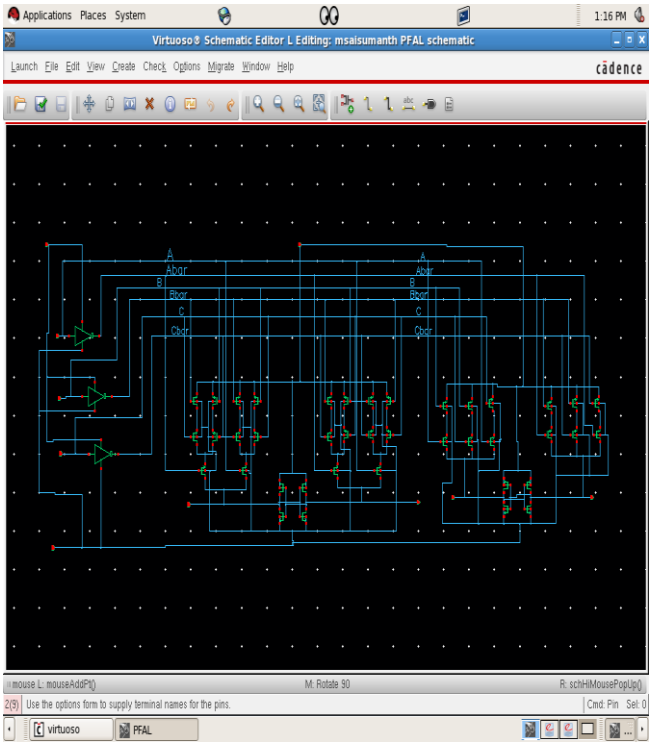

Figure 13: Schematic Of Positive Feedback Adiabatic Logic

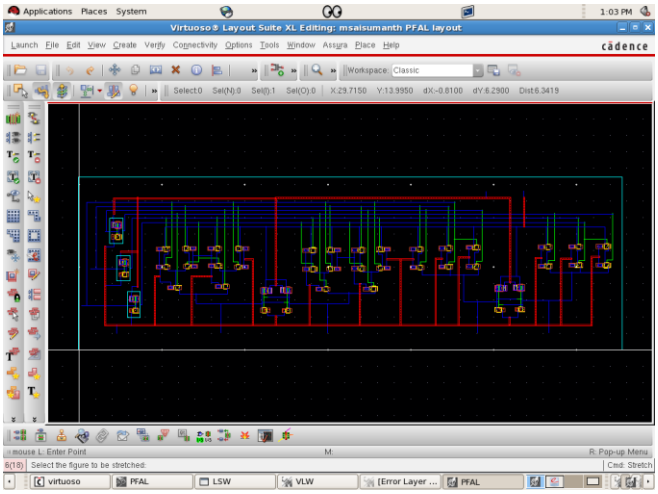

Figure 14: Layout Of Positive Feedback Adiabatic Logic

International Journal of Recent Development in Engineering and Technology
Website: www.ijrdet.com (ISSN 2347-6435(Online) Volume 3, Issue 1, July 2014)

TGAL: The schematic design of Transmission gate based adiabatic logic (TGAL) sum and carry blocks are shown in fig 15 and fig 16. Its layout is shown in fig 17. The general block diagram of transmission gate based adiabatic logic consists of two functional blocks F and complement of F operated with single clock power supply. Both normal and complemented inputs are available to functional blocks. Functional blocks are implemented using transmission gate or pass gate.

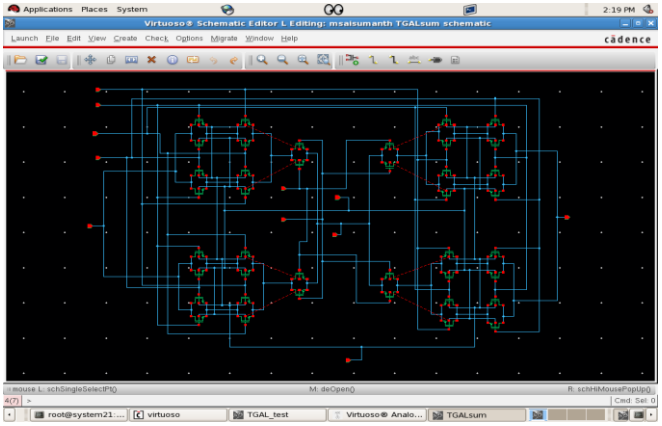

Figure 15: Schematic Of Tgal Sum Block

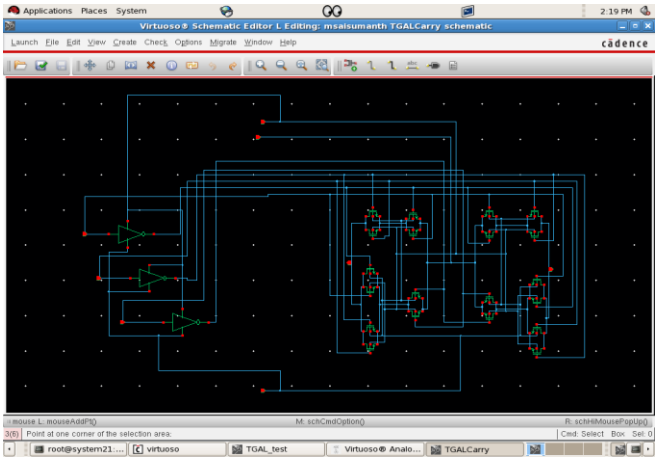

Figure 16: Schematic Of Tgal Carry Block

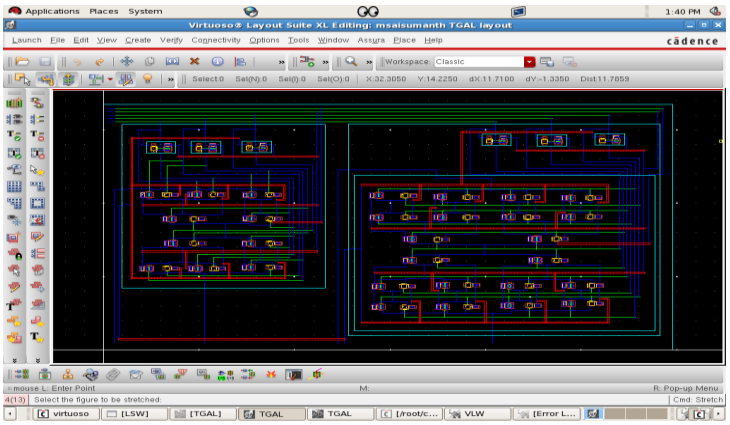

Figure17: Layout Of Transmission Gate Adiabatic Logic

E. SERF Adder [1]

The schematic design of Static Energy Recovery Full Adder and its layout are shown in fig 18 and fig 19. In this adder the energy recovering logic reuses charge and therefore consumes less power than non-energy recovering logic. The circuit consists of two XNORs realized by 4 transistors. Sum is generated from the output of the second stage XNOR circuit. Carry can be calculated by multiplexing **a** and **cin** controlled by (**a** ⊗ **b**).

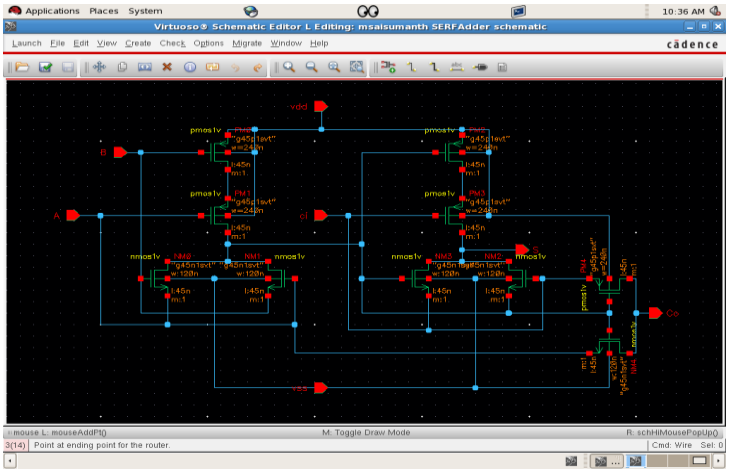

Figure 18: Schematic Of Serf Adder

International Journal of Recent Development in Engineering and Technology
Website: www.ijrdet.com (ISSN 2347-6435(Online) Volume 3, Issue 1, July 2014)

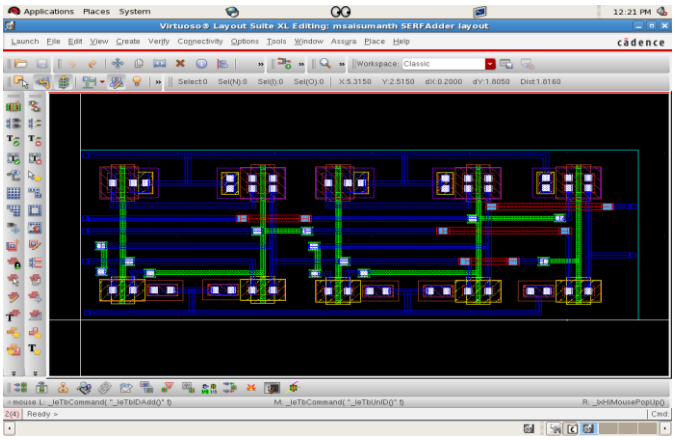

Figure 19: Layout Of Serf Adder

It should be noted that the new SERF adder has no direct path to the ground. The elimination of a path to the ground reduces power consumption. The charge stored at the load capacitance is reapplied to the control gates. The combination of not having a direct path to ground and the re-application of the load charge to the control gate makes the energy-recovering full adder an energy efficient design.

F. Kogge-stone Adder [9]

The schematic diagram of kogge-stone adder and its layout are shown in fig 20 and fig 21. It is one type of sparse tree adder. Kogge-Stone adders are the fastest prefix tree in theory. For *N*-bit addition operation, it has only log2*N* levels to produce the propagate and generate signals. However, the large number of carry merge blocks (*N*log2*N*-*N*+1) lead to cost in layout area and power dissipation.. It mainly consists of three blocks. They are: Pre-processing, Carry look-ahead network, Post-processing.

- Pre-processing produces p= A⊕B and g=A.B
- Carry look ahead network block produces
  Pi:j = Pi:k+1.Pk:j and Gi:j = Gi:k+1 + (Pi:k+1. Gk:j)
- Post-processing block produces
  Sum= Pi ⊕ c_{i-1} and carry= Gi + (Pi . Cin)

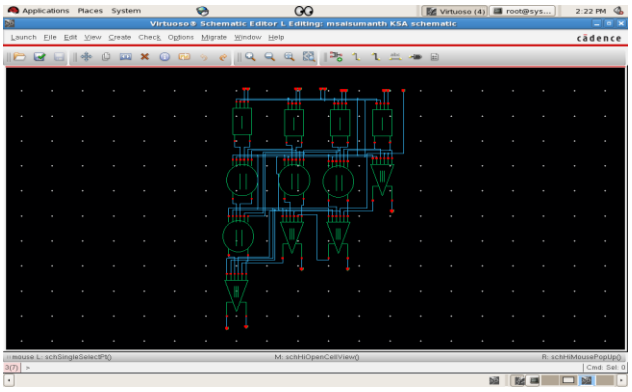

Figure 20: Schematic Of Kogge-Stone Adder

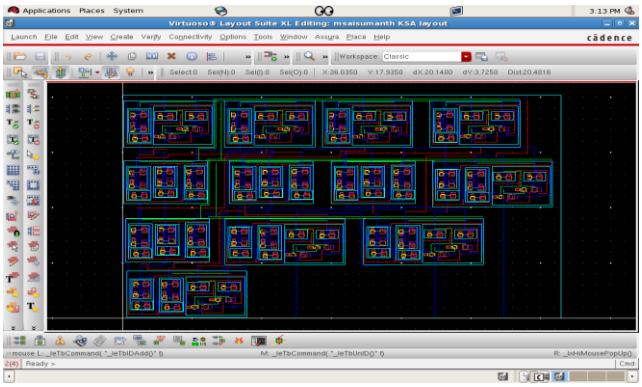

Figure 21: Layout Of Kogge-Stone Adder

IV. Simulation And Analysis

A. Simulation Environment

The proposed ten types of various full adders are simulated and Layout is constructed using virtuoso in Cadence tools. All the results are obtained in 45nm CMOS technology with different supply voltages and at different input signal frequencies.

International Journal of Recent Development in Engineering and Technology
Website: www.ijrdet.com (ISSN 2347-6435(Online) Volume 3, Issue 1, July 2014)

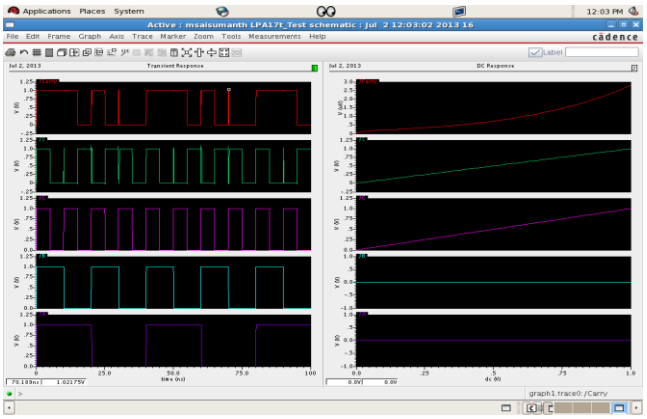

Figure 22: Timing Waveform Of Adder

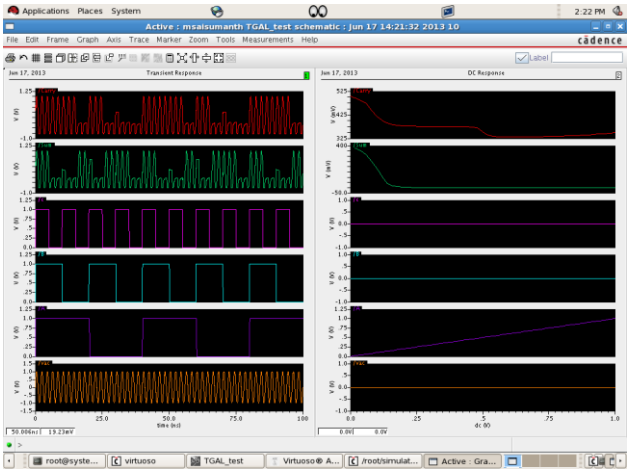

Figure 23: Timing Waveform Of Adiabatic Adders

B. Comparison

Power consumption and working speed (frequency and delay) are yardsticks for the performance of CMOS circuits. These are listed in TABLE 1 to 10 comparisons of ten proposed full adders frequencies and supply voltages.

Another important standard for CMOS circuits is Power-Delay product (*P*DP). This parameter is applied often in testing characteristics of CMOS circuits. Since many cases, requirements of low power and high speed cannot be accomplished simultaneously; comparisons only using these two metrics may become problematical.

TABLE I: PDP ANALYSIS OF 32-BIT BASIC ADDER

Layout Power-delay Product(f W-S)			
Supply Voltage(v)	Frequency(M Hz)		
	100	250	500
0.8	214.11	580.69	922.49
1.0	408.29	877.83	1488.13
1.2	662.00	1295.40	2101.95

TABLE II: PDP ANALYSIS OF 32-BIT FAST ADDER

Layout Power-delay Product(f W-S)			
Supply Voltage(v)	Frequency(M Hz)		
	100	250	500
0.8	104.14	255.51	434.74
1.0	208.58	452.11	745.32
1.2	355.69	779.45	1275.32

TABLE III: PDP ANALYSIS OF 32-BIT 22T ADDER

Layout Power-delay Product(f W-S)			
Supply Voltage(v)	Frequency(M Hz)		
	100	250	500
0.8	58.11	104.44	157.41
1.0	653.97	1010.32	1587.5
1.2	1162.40	1823.40	2515.02

TABLE IV: PDP ANALYSIS OF 32-BIT 17T ADDER

Layout Power-delay Product(f W-S)			
Supply Voltage(v)	Frequency(M Hz)		
	100	250	500
0.8	77.99	196.94	340.28
1.0	131.79	320.51	554.59
1.2	221.53	481.37	828.13

TABLE V: PDP ANALYSIS OF 32-BIT 14T ADDER

Layout Power-delay Product(f W-S)			
Supply Voltage(v)	Frequency(M Hz)		
	100	250	500
0.8	60.37	157.79	265.40
1.0	144.19	302.19	465.01
1.2	249.24	516.95	827.63

International Journal of Recent Development in Engineering and Technology
Website: www.ijrdet.com (ISSN 2347-6435(Online) Volume 3, Issue 1, July 2014)

TABLE VI: PDP ANALYSIS OF PASS TRANSISTOR ADIABATIC LOGIC ADDER

Layout Power-delay Product(f W-S)			
Supply Voltage(v)	Frequency(M Hz)		
	100	250	500
0.8	3.24	3.93	4.55
1.0	242.47	244.04	245.47
1.2	1095.27	1097.96	1105.47

TABLE VI: PDP ANALYSIS OF POSITIVE FEEDBACK ADIABATIC LOGIC

Layout Power-delay Product(f W-S)			
Supply Voltage(v)	Frequency(M Hz)		
	100	250	500
0.8	895.78	898.28	903.52
1.0	948.46	953.74	959.42
1.2	935.22	939.78	951.11

TABLE VIII: PDP ANALYSIS OF 32-BIT TRANSMISSION GATE BASED ADIABATIC ADDER

Layout Power-delay Product(f W-S)			
Supply Voltage(v)	Frequency(M Hz)		
	100	250	500
0.8	984.08	1325.95	1980.81
1.0	1689.39	2184.76	3264.79
1.2	2540.14	3276.29	4838.28

TABLE IX: PDP ANALYSIS OF 32-BIT KOGGE-STONE ADDER

Layout Power-delay Product(f W-S)			
Supply Voltage(v)	Frequency(M Hz)		
	100	250	500
0.8	297.12	867.28	1478.09
1.0	524.48	1086.61	2575.75
1.2	857.24	1630.67	2564.70

TABLE X: PDP ANALYSIS OF 32-BIT SERF ADDER

Layout Power-delay Product(f W-S)			
Supply Voltage(v)	Frequency(M Hz)		
	100	250	500
0.8	45.17	111.32	177.22
1.0	88.73	206.33	334.06
1.2	208.48	399.66	576.18

V. CONCLUSION

In this paper ten types of adders are designed, simulated and layouts are also designed. Designed layouts are simulated with and without RC parameters. According to those analysis these ten adders were compared with each other up to 32-bit and decided that SERF adder is better in all for designing any type of circuit as it is consisting of low power consumption and it also acquires low area as transistor count is less when compared with others.

REFERENCES

[1] "Power and delay comparison between different types of circuits". ISSN 2278-8875, Volume 1, Issue 3, September 2012.

[2] "Performance analysis of Low power full adder cells using 45nm CMOS technology". ISSN 2250-2459, Volume 4, Issue 1, January 2014.

[3] "Comparative analysis of conventional CMOS and energy efficient adiabatic logic circuits". ISSN 2250-2459, Volume 3, Issue 9, September 2013.

[4] "Design of energy efficient full adder using hybrid CMOS logic style". ISSN 2231-1963, Volume 2, Issue 1, January 2012.

[5] "An efficient adiabatic circuit design approach for low power applications". Volume 2, No.1, November 2009.

[6] "Power efficient VLSI inverter design using adiabatic logic and estimation of power dissipation using VLSI-EDA tool". IJCCT. Volume 2, Issue 2,3,4; December 2010.

[7] "A new full adder cell for low power applications". A.M. shams, M.A. Bayougi.

[8] "CMOS/BiCMOS ULSi Low Voltage, Low Power". Kiat-seng Yeo, Samir s. Rofail, Wang-Ling Goh.

[9] "8-bit kogge stone Adder report". Anurag Sindhu, Ashish Bhatia.