Design and Implementation of Different Generations of Current Conveyor using 100nm CMOS Technology

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Abstract— **Current conveyors are unity gain analog building block having high linearity, wide dynamic range and provide higher gain-bandwidth product. The current conveyors operate at low voltage supplies and consume less power. It has high input impedance, low output impedance and unity current gain (Iz/Ix=±1) as well as unity voltage gain (Vx/Vy=1). The working principle of Current Conveyors is very simple. The current conveyors can easily be implemented using voltage follower and current mirrors.**

The proposed current conveyors are simulated using 100nm CMOS technology on Advanced Design System. The main features of these current conveyors are low voltage, less power, high slew rate and wide bandwidth for voltage transfer (Vy to Vx) and current transfer (Ix to Iz) which make them suitable for high frequency and low power applications.

Keywords— **CCI, CCII, current conveyor, current mirrors, current mode circuit**
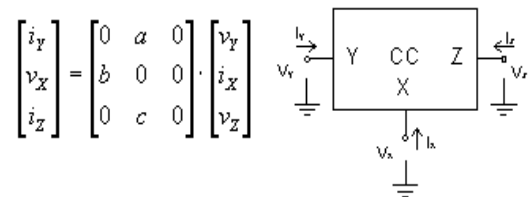
I. INTRODUCTION

The current mode circuits such as Current conveyors (CCs) have received considerable attention and emerged as an alternate building block to the Op-Amp (voltage mode circuit) in the field of analog signal processing [1] due to its potential performance feature. In CCs, the use of current rather than voltage as the active parameter can result in higher usable gain, accuracy and bandwidth due to reduced voltage excursion at sensitive nodes [2]. The current conveyors are not only useful for current processing, but also offer certain important advantages in voltage processing circuits. The nonlinear circuits and dynamics [3] can easily be developed using CCs.

With the reduction in the supply voltage and device threshold voltage of CMOS technology, the performance of CMOS voltage mode circuits has greatly affected which results in a reduced dynamic range, an increased propagation delay and reduced noise margins. The CCs have simple structure, wide bandwidth and capability to operate at low voltage. It also offer unity current gain, unity voltage gain, higher linearity, wider dynamic range and better high frequency performance.

II. THE CURRENT CONVEYORS

The current conveyor is an active building block which is used in implementation of analog circuits and systems. It was firstly introduced by Sedra A and Smith K C [4] in 1968. Subsequently in 1970, they had reformulated it as second generation Current conveyor called CCII [5]. In the recent years, CCII have become very useful for implementation of analog signal processing circuits such as amplifiers, oscillators, filters and nonlinear circuits. The current conveyor is functionally flexible and versatile in nature as it has precise unity voltage gain between X and Y; unity current gain between Z and X (fig. 1), rather than the high ill-defined open loop gain of Op-Amps. Because of this fact, CCII is generally used without feedback in amplifier applications [6, 7].

The build block of current conveyor and its generalised characteristics equation is shown in fig.1. The current conveyor is a grounded three-port network represented by the black box (fig 1) with the three ports denoted by X, Y, and Z. Its terminal characteristics can be represented best by a hybrid matrix giving the outputs of the three ports in terms of their corresponding inputs [8].

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & a & 0 \\ b & 0 & 0 \\ 0 & c & 0 \end{bmatrix} \cdot \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix}$$

Fig 1: Building block of Current conveyor with characteristics matrix

Here a, b and c are generalized coefficients and these can have any value form -1 either 0 or +1.

III. FIRST GENERATION CURRENT CONVEYOR

The first generation Current Conveyor (CCI) is characterized by port relation [4], expressed by matrix equation (1).

$$\begin{vmatrix} I_y \\ V_x \\ I_z \end{vmatrix} = \begin{vmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{vmatrix} \begin{vmatrix} V_y \\ I_x \\ V_z \end{vmatrix} \quad \text{…………..(1)}$$

From eq. (1) ---

- It is stated that a voltage is applied to terminal Y, an equal potential will appear on the terminal X. (i.e. $V_x = V_y$.)
- An input current I_x being forced into terminal X will result an equal amount of current into terminal Y and the same amount of current will be conveyed to output terminal Z.
- Potential at X being set by Y is independent on the current being forced at X. Similarly current through port Y being fixed by X is independent on the applied voltage to Y.

CMOS Implementation: - The first characteristic (ie $V_x = V_y$) is implemented using voltage follower and second characteristic (ie $I_y=I_x$ & $I_z=I_x$) is implemented using current mirrors as shown in fig. 2.

This is class-A configuration. Where NMOS transistors M1 and M2 form a current mirror that forces the drain currents of the PMOS transistors M3 and M4 to be equal and hence the voltages at terminal X and Y are forced to be equal. The current mirror formed by M1, M2 and M5 with input Ix, forced to drain of M2 provides equal amount of current is being conveyed at drain of M5.
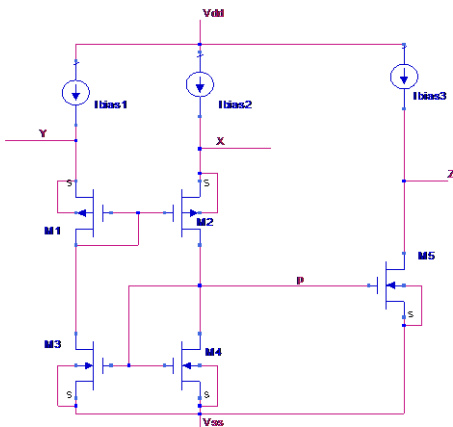
Fig 2: Circuit diagram of CCI – class A

The major problem in this circuit is only unidirectional current is being conveyed at Z terminal. To overcome this problem Class-AB configuration is preferred. The Push-pull topology based Class-AB CCI circuit is capable of bidirectional current operation [9].

This is implemented using two complementary conveyors of class-A type as shown in fig. 3.
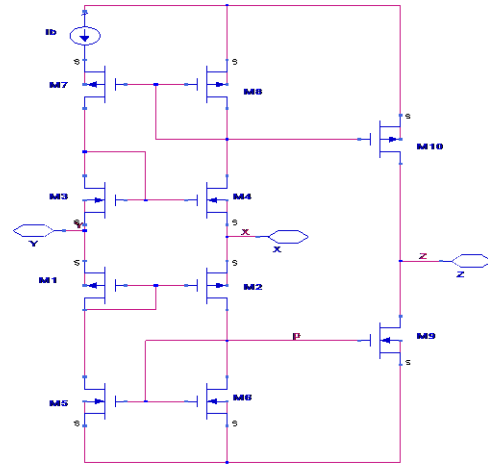
Fig. 3: Circuit diagram of CCI – class AB

The major problem in CCI is its low input impedance at 'Y'; the voltage input port which causes loading to the preceding stage or input

IV. SECOND GENERATION CURRENT CONVEYOR

The second generation current conveyor (CCII) is one of the most versatile current-mode building block for many applications. It offers high input impedance at voltage input port 'Y', which is preferable in order to avoid loading effect. So, second generation current conveyor is developed to overcome the problem loading effect of CCI. The CCII is considered as a basic building block in analog circuit design because all the analog applications can be developed by making suitable connections of one or more CCIIs with passive and active components.

It is a three terminal device and the block representation similar to the Generalized Current Conveyor as shown in fig (1).

The second generation Current Conveyor (CCII) is characterized by port relation, expressed by matrix equation (1).

$$\begin{vmatrix} I_y \\ V_x \\ I_z \end{vmatrix} = \begin{vmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm1 & 0 \end{vmatrix} \begin{vmatrix} V_y \\ I_x \\ V_z \end{vmatrix} \quad \text{…(2)}$$

From eq. (2) ---

- It is stated that a voltage is applied to terminal Y, an equal potential will appear on the terminal X. (i.e. Vx = Vy.)
- An input current Ix being forced into terminal X will result in an equal amount of current conveyed to output terminal Z.
- Potential at X being set by Y is independent on the current being forced at X.

The port X can be used as a voltage output or as current input port. Therefore, this current conveyor can be used to process both voltage and current signals.

The input/output impedance levels of all three terminals/ports [10] are as follows.

TABLE I
IMPEDANCE LEVEL AT CCII PORTS

| CCII Port	Type of Port	Impedance level	Remark
X	Current input Voltage output	Low (Ideally Zero)	Best for current input and voltage output port as IR drop is very less (ideally Zero)
Y	Voltage input	High (Ideally Infinite)	Avoids loading of preceding stage.
Z	Current output	High (Ideally Infinite)	It will provide constant current and not get loaded even from succeeding stage having poor input impedance.

There are two types of second generation current conveyors:

- Positive Current conveyor (CCII+) in which the current Ix and Iz are in phase.
- Negative Current conveyor (CCII-) in which the current Ix and Iz are 180^0 out of phase.

The derivative these two current conveyor is Dual Output Current Conveyor (DOCC) which provides both types of output currents, Iz+ (in phase with Ix: CCII+) and Iz- (180^0 out of phase with Ix: CCII-)

CMOS Implementation: - There are two possible topologies for implementation of second generation current conveyor. Those are class A and class AB. The class AB [11] is provides bidirectional current output, better bandwidth and stable voltage/current gain than class A. Thus here only class AB topology is considered for implementation.
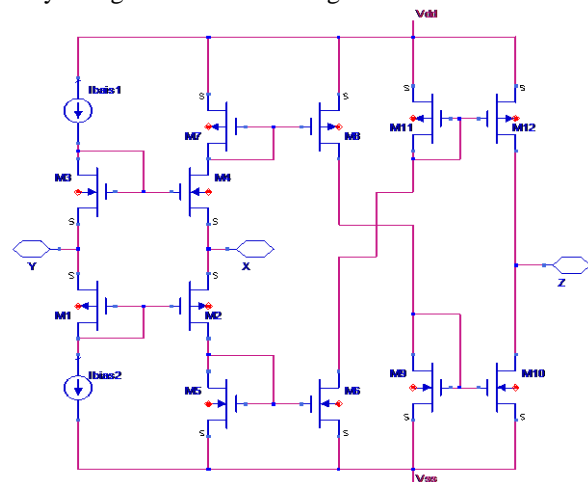
The class AB topology of positive second generation current conveyor is shown in fig 4.
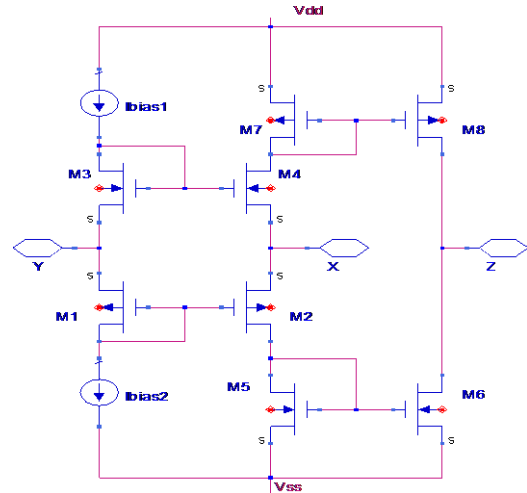
Fig 4: Circuit diagram of CCII+

To ensure the correct operation the bias current Ibais1 and Ibais2 have to be equal; in order to set the quiescent current IB. In this circuit, the current flow through X is nonlinearly divided in two signal path through either NMOS or PMOS current mirror which is summed at port Z.

The class AB topology of second generation current conveyor negative is shown in fig.5.


Fig 5: Circuit diagram of CCII-

To ensure the correct operation the bias current Ibais1 and Ibais2 have to be equal; in order to set the quiescent current IB.

In this circuit, the current flow through X is nonlinearly divided in two signal path through either NMOS or PMOS current mirror; those are cross coupled with another PMOS and NMOS current mirror respectively. Because of these addition current mirrors current at Z becomes 180^0 out of phase with Ix.

The Dual Output class AB second generation current conveyor has been implemented using a voltage follower VF1 which is biased with current I_1 and I_2. Where the bias current I_1 and I_2 are equal; in order to set the quiescent current IB. In this circuit, the current flow through X, I_x is nonlinearly divided in two signal path through either dual output current mirror CM1 (NMOS) or CM2 (PMOS). The port Z+ is obtained by directly connecting one output CM1 to one output of CM2 so as to sum up the nonlinearly divided current. The port Z- is obtained by cross coupling of CM1 with CM4 (PMOS), CM2 with CM3 (NMOS) and direct coupling of CM3 with CM4, as shown in fig 6. Because of this cross coupling current at Z- port becomes 180^0 out of phase with I_x.
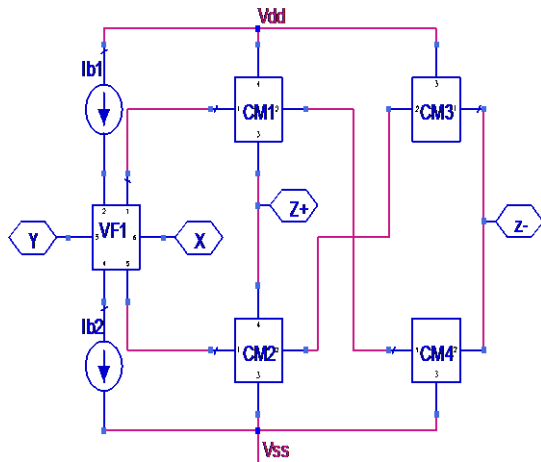
**Fig. 6 Block Diagram of Dual output CC**

V. RESULT AND DISCUSSION

To validate the theoretical concept as expressed by matrix equations (eq. (1) and eq. (2)) and CMOS implementation as shown in fig (2), (3), (4), (5), (6) is simulated using Advanced Design System. For simulation supply voltage of ±2v and 100nm technology is used. These simulation results studied in depth.

Here only CCII- is considered for discussion, hence all the characteristics and input-output waveforms shown are related to CCII-. From fig (7) Voltage transfer characteristic and fig (8) Current transfer characteristic, it is observed that it provide unity voltage and current gain. From Frequency response shown in fig (9A) and fig (9B), it is observed that it provides wider current and voltage bandwidth. It is also observed that it provide constant unity voltage gain and constant unity current gain over wide range of frequency. The transient response with step input excitation is shown in fig (10A); from this response it is observed that output needs certain settling time. Similarly with sine wave input excitation of 10GHz, the transient response of fig (10B) shows that output voltage V_X is not in phase with input voltage V_y and initially V_x is zero for certain duration though the voltage gain is unity that is magnitude of V_x and V_y are equal. This phase lag is introduced due to propagation delay which is negligibly small.

The different parameter of negative CCII class-AB topology was studied and findings are tabled below.

TABLE III
**DIFFERENT PARAMETERS OF CCII-**

| Sr. No.	Parameter		CCII-
1	Operating Voltage		±2V
2	Bias Current		10uA
3	Current Gain		1
4	Voltage gain		1
5	Current bandwidth		1.65 THz
6	Voltage bandwidth		2.5THz
7	Power consumption		29.7uW
8	Propagation delay for		
	Current Transfer	Sine wave	68fsec
		Square wave	350fsec
	Voltage transfer	Sine wave	< 1fsec
		Square wave	< 1fsec
9	Port Impedance	X	< 1mΩ
		Y	< 1mΩ
		Z	> 1TΩ
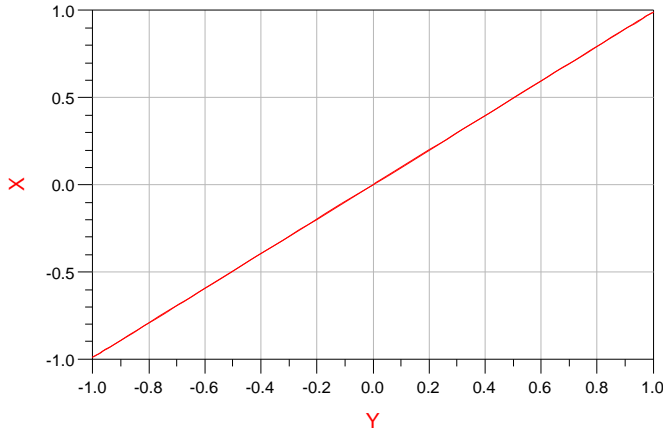
Fig 7: Voltage transfer characteristic
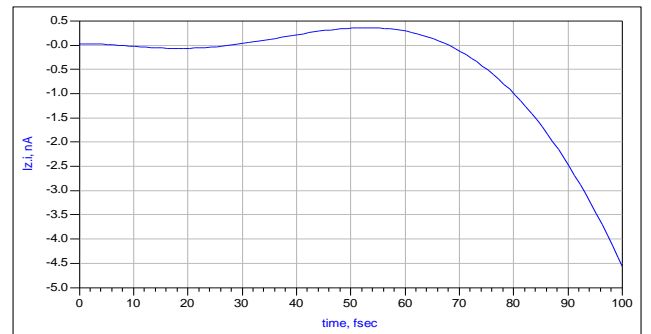

Fig 8: Current transfer characteristic

m1
freq=1.650THz
(Iz.i/Ix.i)=0.707 / 84.089
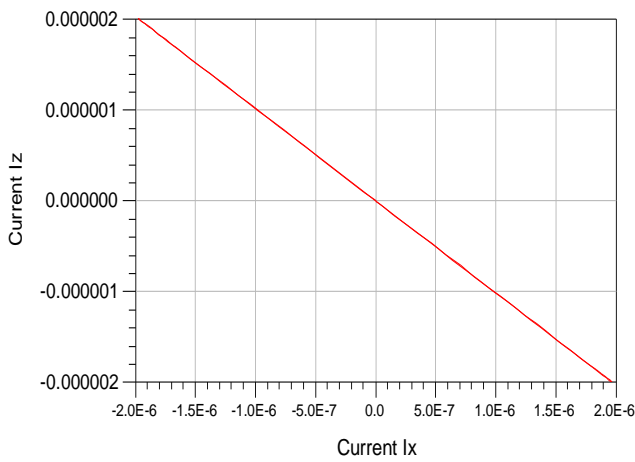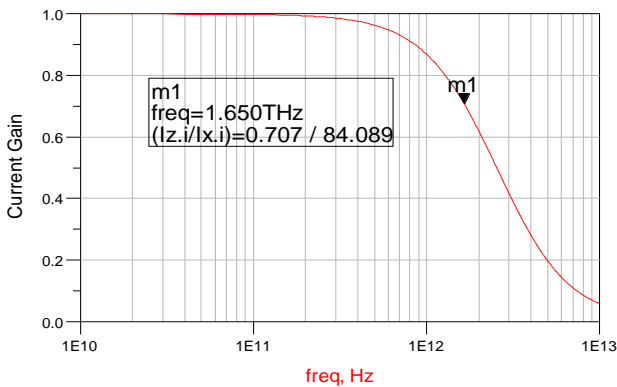
Fig 9A: Frequency Response of current

m1
freq=2.500THz
X/Y=1.000 / -0.004
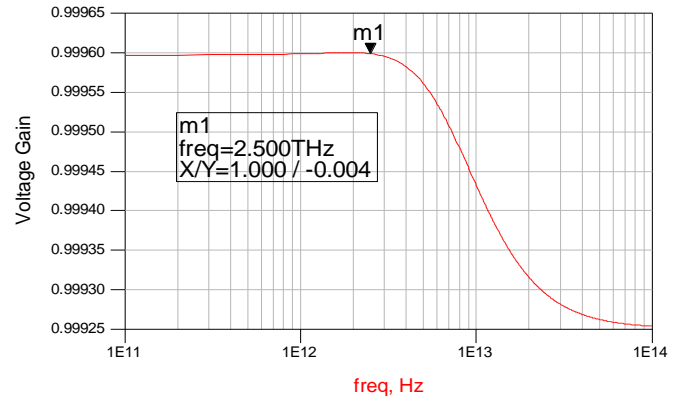
Fig 9B: Frequency Response of Voltage
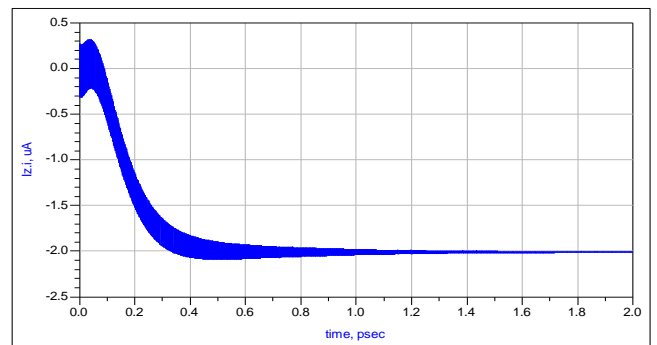
Fig. 10A: Transient Response of setup input

Fig.10B: Transient Response of sine wave input

VI. CONCLUSION

The Class AB topology of all derivatives of CCI and CCII operates at wide range of supply voltage and consumes less power. These current conveyors provide unity current gain and unity voltage gain over a wide range of frequency; in other word they have a broader bandwidth.

These current conveyors don't have a problem of propagation delay which introduces negligibly small phase lag. At lower frequency signal this phase log is almost zero. Even at higher frequency it has very small value for current transfer and almost zero for voltage transfer. In a single stage analog system working up-to 1THz, the propagation delay is insignificant. But in multi stage (10 or more stages) cascading system and/or working above 1THz, the propagation delay may create some anomaly. Being an analog system the propagation delay is not a serious issue, unlike in digital system.

Lastly it is concluded that second generation Current conveyor is best building block in analog system design and development.

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