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A 45-nm CMOS 16-bit Segmented Current-Steering Digital-to-Analog Converter

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***Abstract*—This Paper presents a 16-bit Digital-to-Analog Converter (DAC) using 45 nanometer CMOS technology for mixed-signal applications. A segmented current steering architecture is used for this DAC in which 6-bits are used in thermometer coded architecture while 10-bits are used in binary weighted architecture. This architecture gives the most optimized results in terms of speed, resolution and power. The designed 16-bit DAC operates with two supply voltages, 1 V and 3.3 V. The designed 16-bit DAC provides acceptable accuracy with Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) of ± 0.8 Least Significant Bit (LSB) and ± 0.7 Least Significant Bit (LSB), respectively. The measured Spurious Free Dynamic Range (SFDR) at 1 GHz sampling rate is 68 dB. The average power dissipation at 1 GHz sampling rate is 2.74 mW. The maximum sampling rate of DAC is 1.62 GHz. The tool used for simulation is Tanner S-Edit and T-Spice.**

***Keywords*— Binary Weighted, CMOS Analog Circuits, Current Steering, Digital to Analog Conversion, Mixed Analog -Digital Integrated Circuits.**

I. INTRODUCTION

This With the advances in VLSI (Very Large Scale Integration) technology, digital signal processing is penetrating into more and more applications. Many applications which have been implemented in analog domain have been moved to digital, such as wireless cellular phones. Most of the integrated circuits have both analog and digital circuits. This is called mixed-signal integration. The analog and digital integrated circuits were designed and fabricated in different technologies. Usually, analog circuits use bipolar technologies, while digital circuits are in MOS (Metal Oxide Semiconductor) technologies.

CMOS technology dissipates less power compare to other design. CMOS architecture can be easily scaled down for the major three factors: 1) Area 2) Speed 3) Power [01]. Furthermore, CMOS circuits proved to have a low fabrication cost. The low cost of fabrication and the possibility of placing both analog and digital circuits on the same chip so as to improve the overall performance and/or reduce the cost of packaging made CMOS technology attractive.

Thus CMOS technologies become mainstream technologies for mixed-signal integration due to the advantages of high speed, low power and high integration density. Over the past three decades, CMOS technology scaling has been a primary driver of the electronics industry and has provided a path toward both denser and faster integration. The transistors manufactured today are 20 times faster and occupy less than 1% of the area of those built 20 years ago [1].

Digital systems have enormous advantages over analog systems like accuracy, speed, immunity to noise, etc. With advent growth of VLSI technology, digital systems have become more sophisticated, more powerful and more reliable than ever before. But one point that needs to be remembered forever is that "The Real World is Analog". Thus, to take advantages of digital systems, we need to convert real world analog signals to digital signals and after processing them, we need back conversion to obtain real world outcome. This phenomenon has led to development of data converters – A/D and D/A Converters.

In electronics, a Digital-to-Analog converter (DAC or D-to-A) is a device that converts a digital (usually binary) code to an analog signal (current, voltage, or electric charge). Signals are easily stored and transmitted in digital form, but a DAC is needed for the signal to be recognized by human senses or other non-digital systems.

A common use of digital-to-analog converters is generation of audio signals from digital information in music players [2]. Digital video signals are converted to analog in televisions and cell phones to display colours and shades. Digital-to-analog conversion can degrade a signal, so conversion details are normally chosen so that the errors are negligible.

Due to cost and the need for matched components, DACs are almost exclusively manufactured on Integrated Circuits (ICs) [2]. There are many DAC architectures which have different advantages and disadvantages. The suitability of a particular DAC for an application is determined by a variety of measurements including speed and resolution.

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II. DAC ARCHITECTURES

A Particularly all the high speed D/A converters are based on the current steering architecture due to its capability of driving resistive loads without buffering. This architecture also provides good static characteristics with reduced power dissipation and area. But the main disadvantage with this architecture is the rapid increase in harmonic distortion caused by the glitches generated from the current switches when the signal frequency is increased [4].

The current steering architecture can be implemented by either binary or unary architecture. In this paper an attempt has been made to optimize the segmentation between the unary and binary implementation in this architecture so to achieve a good linearity with reduced power and area [3].

III. SEGMENTED CURRENT-STEERING ARCHITECTURE

All The binary-weighted (or binary-encoded or binary-scaled) DAC utilizes a number of elements (current sources, resistors, or capacitors) that are binary weighted. One of the drawbacks with the binary-weighted architecture is that for a larger number of bits, the difference between the MSB and LSB weights is large and the DAC becomes sensitive to mismatch errors and glitches [08]. If the matching errors are too large, monotonicity cannot be guaranteed. A solution to minimize the influence of these problems is to encode the binary code into a thermometer code [9]. The advantage with the binary-weighted DAC is that the number of switches and digital encoding circuits is kept at a minimum.

The thermometer-coded DAC architecture utilizes a number of equal size elements. The binary input code is encoded into a thermometer code. Generally, with N binary bits, we have $M = 2^N - 1$ thermometer bits.

Typically, the thermometer-coded DAC architecture is used for low resolutions, say $N < 8$, since otherwise the encoding circuits becomes too large [11]. For a larger number of bits, the digital circuits converting the binary code into thermometer code and the number of interconnecting wires grow exponentially [09].

Usually, to leverage the clear advantages of the thermometer-coded architecture and to obtain a small area simultaneously, a compromise is found by using segmentation [5]. The DAC is divided into two sub-DACs, one for the MSBs and one for the LSBs. Thermometer coding is used in the MSB where the accuracy is needed most [10]. Because of the reduced number of bits in this section, the size is considerably smaller than a true thermometer coded design.

The LSB section can either be done using the binary-weighted or the thermometer-coded approach. We will refer to a fully binary-weighted design as 0% segmented, whereas a fully thermometer-coded design is referred to as 100% segmented [10].

IV. DAC BUILDING BLOCKS

Figure 1 shows the block diagram for the "$(N-B)_{(MSB)}$ + $B_{(LSB)}$" segmentation. The digital inputs are first clocked into input registers. Then the first (N-B)/2 MSB's are column decoded, the next (N-B)/2 bits are row decoded, and the final B bits are sent to the decoding logic for the B-bit LSB section. The LSB section is implemented by binary weighted current cells. The main building blocks in this prototype are the unit current cells, the biasing for the current cells and the thermometer decoder design.

A. Unit Current Cell

The current cell configuration used here is a thick oxide layer transistor for the switch cascode [12].

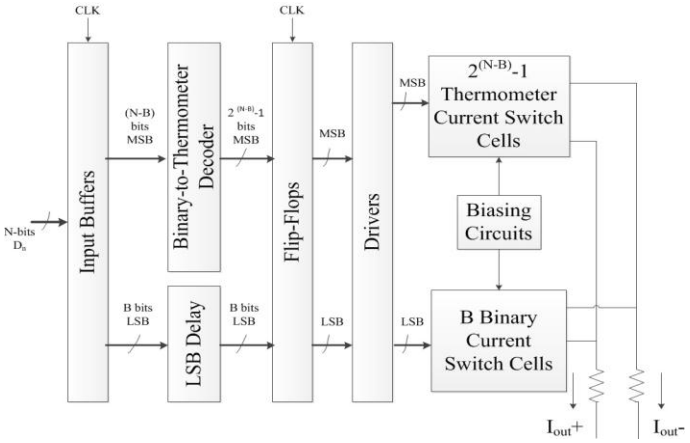

Figure 1 - Block Diagram of Segmented Architecture

This thick oxide layer transistor can operate with a higher supply voltage up to 3.3 V. Hence the voltage headroom is increased significantly. Care should be taken to prevent the voltage at the drain of the switching transistors from increasing beyond the maximum supply voltage in 45-nm technology i.e. beyond 1 V. Methods used to keep the voltage at the drain of the switching transistor below 1 V are explained below.

The drain voltage of the switching transistor can be held constant by using a voltage regulator. The voltage regulator (Zener diode) is connected in parallel such that the voltage at the drain remains below 1 V, but its unknown leakage current flows through output of the DAC.

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The output current of the current steering DAC should be proportional to the input code. Hence this unknown current in the output terminal results in improper conversion. An ideal current source of a few µA instead of the regulator can be a solution to have a constant voltage at the drains of the switching transistors. This configuration is illustrated in figure 2.

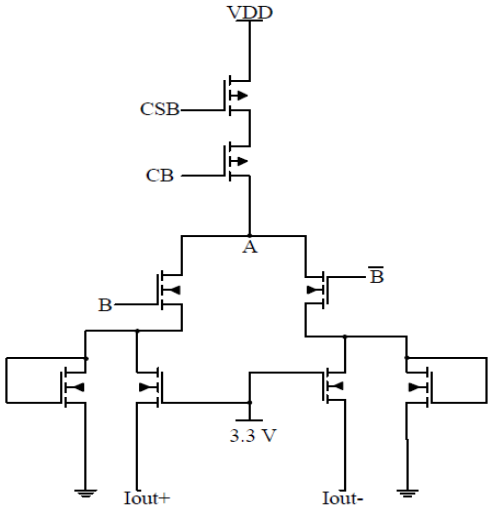

Figure 2 - Cascode Current Source with Thick Oxide Layer Cascoded Switches [12]

B. Binary-to-Thermometer Decoder

The Binary to thermometer decoder is used to convert N bit binary input into $2^N - 1$ Thermometer coded output lines. In this implementation, 6 bits are converted into thermometer code. Thus we need 6 bit binary to thermometer decoder. To reduce the complexity, 6 bit decoder is divided into two 3 bit decoders which are used for raw and column of unary current cell array. The combination of raw and column output is given to individual current cell. The combination logic is shown in figure 3. This combination logic circuit is provided in each current cell [02] [06].

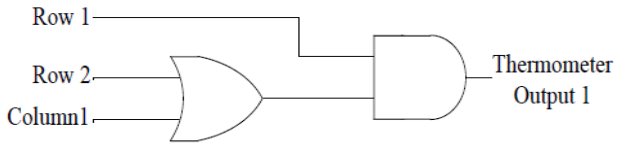

Figure 3 - Row Column Combination Logic

C. Biasing Circuit

This biasing circuit is divided into two parts: global biasing and local biasing. As shown in figure 4, the global biasing is used to bias the local biasing. The global biasing is provided outside the current source array, while the local biasing is provided in all current sources. Using global and local biasing avoids problems with voltage drops across the different interconnects used in the array. The resistor R used in this circuit is off-chip.

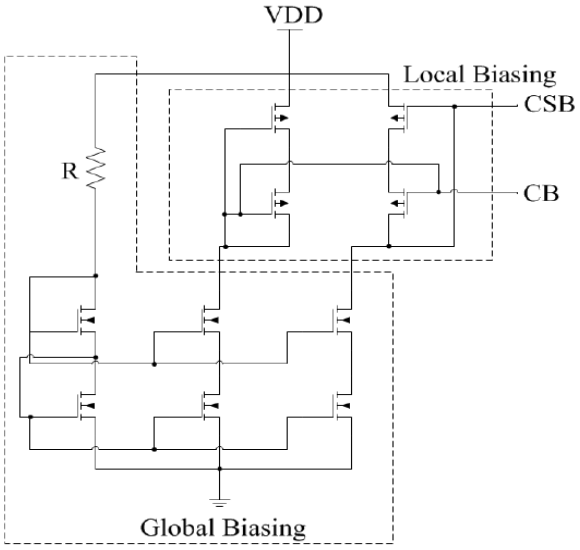

Figure 4 - Cascoded Current Mirror based Biasing Circuit [8]

V. Simulation Results

Figure 5 shows a part of the ramp output of 16-bit DAC. As shown in figure, there are small glitches at the transition from one level to next level. This is because of the binary weighted architecture used in 12 LSBs. However, these glitches can be reduced by using a low pass filter at the output stage of the DAC. Here, simple LC low pass filter is used, but the result can further be improved using active filters. The unit current value is set at 200 nA.

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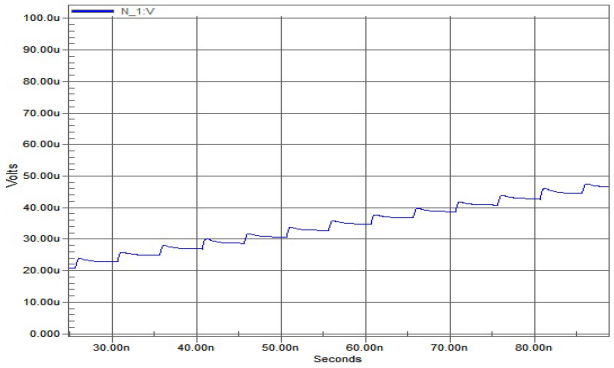

Figure 5 - Ramp Output of 16-bit Segmented DAC

Figure 6 shows reconstructed sine wave output of 16-bit DAC. As compared with the results of 6-bit DAC, the sine wave accuracy becomes higher as the resolution increases. Figure 7 shows the FFT spectrum of sine wave output. From figure 7, the measured SFDR is 68 dB.

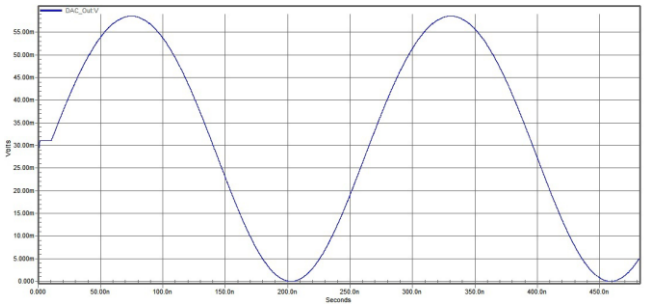

Figure 6 - Reconstructed Sine Wave Output of 16-bit Segmented DAC

Figure 8 shows the DNL and INL plots of 16-bit DAC. As shown, the measured DNL and INL are $\pm$ 0.8 LSB and $\pm$ 0.7 LSB, respectively. Although this does not satisfy the condition for monotonicity, the performance is still acceptable in most applications. The output current range is 0 to 13.11 mA. The measured response time of the DAC is 650 ps and the settling time is 308 ps. The Total Harmonic Distortion (THD) is -38.6 dB and Signal-to-Noise Ratio is 79 dB at sampling frequency of 1 GHz.

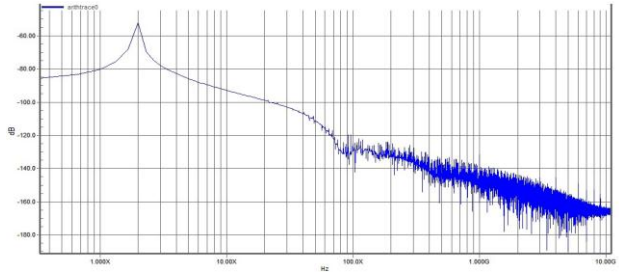

Figure 7 - FFT Spectrum of Sine Wave Output of 16-bit DAC

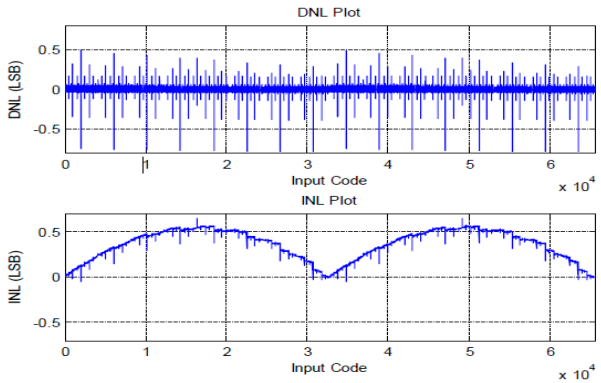

Figure 8 - DNL and INL Plots of 16-bit DAC

VI. Challenges And Future Enhancements

Modern DACs only partially benefit from the recent developments of the CMOS IC processes. While their speeds, e.g. sampling rates and utilized signal bandwidth, are expected to continue rising, their accuracy, occupied silicon area and production costs are expected to remain problematic design bottlenecks.

In current steering DACs, the transistor mismatch limits the accuracy of the signal and bias current sources. These tolerances translate to mismatch among the parallel current cells, causing DAC static and dynamic non-linearity. For good transistor matching, the transistors need to be made big and laid out close to each other. Other performance limitations include clock-feedthrough, data-feedthrough, data-dependent disturbances of the substrate and power rails, systematic parasitic due to the layout, output glitches, etc. When these errors are data-dependent, they cause Harmonic Distortion (HD) of the input signal and hence limit the DAC linear performance.

However, various correction methods are available to counteract these performance limitations. These correction methods may support the DAC performance in various ways, e.g. improve overall intrinsic performance, improve chip yield, relax and improve particularly targeted design specifications. Moreover, the evolution of the IC technologies favour the development of sophisticated correction methods, since the chip co-integration price per function becomes low. This argument is particularly plausible for digital correction methods and introduces the trend of digitally assisted analog performance.

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VII. Conclusion

As shown by the results, the implemented DAC provides desired level of accuracy with moderate power consumption. In any applications with the requirement of high speed and accuracy, this DAC can be used.

However, there are some issues that need to be considered with this design. First, in situations where the low power is utmost requirement, this DAC may not be used. The power can be reduced in this design either by using basic current source configuration, or by reducing the current step size. But, both these steps lower down the accuracy of the DAC.

Similarly, if further enhanced accuracy is required, then the calibration techniques must be incorporated in the design. The calibration techniques include dynamic element matching, digital calibration techniques and self-calibration techniques. However, including such techniques may increase the complexity and power consumption of the design. So there is a trade-off between power and accuracy of the DAC. Table I summarizes and compares the simulation results of 16-bit segmented DAC with previous implementations.

TABLE I
Summary and Comparison of Simulation Results of 16-bit DAC Designs

Parameters	This Design	[13]	[14]
Resolution	16-bit	16-bit	16-bit
Technology	45-nm CMOS	90-nm CMOS	0.35-µm TSMC
Supply Voltage	1 V & 3.3 V	1.2 V	3.3 V
Output Current Swing	0 – 13.11 mA	-	-
DNL	± 0.8 LSB	± 1.5 LSB	± 0.1 LSB
INL	± 0.7 LSB	± 2 LSB	± 0.3 LSB
SFDR	68 dB at f_s = 1 GHz	-	-
SNR	79 dB at f_s = 1 GHz	-	-
THD	- 38.6 dB at f_s = 1 GHz	-	-
Average Power Dissipation	2.74 mW at f_s = 1 GHz	1.443 mW at f_s = 50 MHz	165 mW at f_s = 50 MHz
Response Time	650 ps	-	-
Settling Time	308 ps		
Max. Sampling Frequency	1.62 GHz	-	-

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