International Journal of Recent Development in Engineering and Technology
Website: www.ijrdet.com (ISSN 2347 - 6435 (Online)) Volume 2, Issue 3, March 2014)

Minimization of Leakage Power using Process, Voltage and Temperature (PVT) Variations

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***Abstract*— Leakage power has become a serious concern in nanometer CMOS technologies. In this paper to minimize the leakage power a supply voltage and body-bias voltage generating technique for nanoscale VLSI systems are used. The minimum level of VDD and the optimum body-bias voltage are generated for different temperature and process conditions adaptively using a lookup table method based on the PVT monitoring and controlling systems. The adaptive optimal body-bias voltage is generated from the proposed leakage monitoring circuit, which compares the sub threshold current (*I*SUB) and the band-to-band tunneling (BTBT) current (*I*BTBT) along with current comparator & charge pump circuit. . The result is simulated using HSPICE using 32-nm bulk CMOS technology.**

***Keywords*— Leakage power, optimal VBody control, optimal VDD control, process, voltage, and temperature (PVT) variation.**

I. INTRODUCTION

To achieve higher density, higher performance and low power consumption, CMOS devices have been scaled for more than 30 years[2-3].

Leakage current is a major drawback in nanoscale CMOS. Because of the continued scaling of technology and supply-threshold voltage, leakage power has become more significant in power dissipation of nanoscale CMOS circuits. Therefore, estimating the total leakage power is critical to designing low-power digital circuits[4-5].

In nanometer CMOS circuits, the main leakage components are the subthreshold, gate-tunneling and reverse-biased junction band-to-band-tunneling (BTBT) leakage currents. As transistor geometries decrease, it is necessary to reduce the supply voltage to avoid electrical breakdown and obtain the required performance. However, to retain or improve performance, it is necessary to reduce the threshold voltage (Vth) as well, which results in an exponential increase of subthreshold leakage. To control short-channel effect and increase the transistor driving strength in deep-submicron (DSM) circuits, gate-oxide thickness also becomes thinner as technology scales down.

The aggressive scaling in the gate oxide results in a tunneling current through the oxide, which is a strong exponential function of the oxide thickness and the voltage magnitude across the oxide. In scaled devices, the higher substrate doping density and the application of ‘‘halo’’ profiles cause significantly large reverse-biased junction BTBT leakage currents through the drain- and source-substrate junctions[7].

This is a serious problem in portable electronic systems that operate mostly in sleep mode. To minimize leakage power dissipation, researchers have proposed several circuit techniques such as multithreshold-voltage CMOS (MTCMOS) and variable threshold-voltage CMOS (VTCMOS) using variable substrate bias voltage. However, these techniques require significant circuit modification and performance overhead for leakage reduction[10-11].

This chapter included the background study to minimize the leakage power. To minimize the leakage power a supply voltage and body-bias voltage generating technique for nanoscale VLSI systems are used. The adaptive supply voltage V_{DD} are generated for different temperature and process conditions adaptively using a lookup table method and the optimum body-bias voltage are generated by using leakage monitoring circuit along with current comparator & charge pump circuit.

II. RELATED WORK

- To collect the material of VLSI design, process corners and nanometer technology.
- To collect the material of different parameters like process, voltage and temperature.
- To find out all required parameters such as supply voltage, body-bias voltage at different temperatures & processes for different process corners, subthreshold current (ISUB) and the band-to-band tunneling (BTBT) current (IBTBT) for different temperatures.
- Selecting appropriate software such as H-spice used for simulation.

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- Doing the coding of different circuits for simulation.
- To simulate the results of different circuits.
- Plotting of graphs for different circuit parameters.

III. Functional Block Diagram

The block diagram of VDD and VBody control system used to generate novel adaptive supply voltage and body-bias voltage for nanoscale VLSI systems is as shown in fig1.

A novel design method is used to minimize the leakage power during standby mode using a novel adaptive supply voltage and body-bias voltage generating technique for nanoscale VLSI systems. The process, voltage, and temperature (PVT) variations are monitored and controlled independently by their own dedicated systems. The minimum level of VDD and the optimum body-bias voltage are generated for different temperature and process conditions adaptively using a lookup table method based on the PVT monitoring and controlling systems.

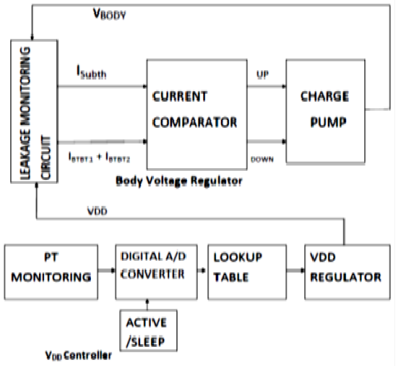

Fig.1: Block Diagram of VDD & VBody control system based on current comparator.

The Block diagram shown in Fig. I consist of following circuits.

- Process/temperature monitoring circuits,
- Digital analog-to-digital(A/D) converter,
- Lookup table with VDD regulator,
- Leakage monitoring circuit,
- Current Comparator,
- Charge pump, and voltage controller including VDD monitoring circuit.

A lookup table is used to characterize the optimal VDD target for various temperature and process conditions detected by the temperature and process monitoring circuits.

The VDD targets for different temperature and process conditions are derived from simulations or direct measurements of the actual die of interest, whereas the body-bias voltages for nMOSFET and pMOSFET are set automatically by the control system to ensure that the chip dissipates a minimal power in standby (sleep) mode. For the most accurate tabulation of the optimal VDD choices for a given process corner and temperature, measurements would have to be performed on each chip. Even if the lookup table is not fully tabulated by completely characterizing the chip for all the possible conditions, the VDD/VBody scaling results are still acceptable, because the body bias controller compensates adaptively for the parameters variations by adjusting the body-bias voltage directly and continuously.

The power-supply voltage is set in the open-loop system, and the body-bias voltage is set and controlled by the closed-loop system including body-bias controller. Reverse body biasing (RBB) is often used to reduce the leakage power in MOS transistors. However, the recent research has shown that if this RBB is too high, the leakage power can be actually increased due to the contribution of the BTBT currents. Therefore, this system proposes a new optimal BBS to balance the sub threshold leakage with the BTBT leakage as explained in the previous section.

The proposed system increases Vth by adjusting the body-bias voltage in the RBB direction so as to reduce the sub threshold-leakage current. When the optimum body point is detected, the body-bias voltage adjustment is stopped to avoid excessive reverse body bias. Although the leakage monitoring circuits are mentioned in], their circuit-models do not extract exact sub threshold leakage and BTBT leakage components in the replica circuit.

In Fig.1, the body bias voltage generator consisting of leakage monitoring circuit, current comparator and a charge pump are used to detect the optimal body-bias voltage. The circuit uses current-mode circuit technique to process the active signals in the current domain, and it offers a number of advantages such as better sensitivity, high speed, and low-power dissipation.

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IV. Programming And Results

1. Temperature Monitoring Circuit:

Algorithm:

1. Start
2. Select process corner choice.

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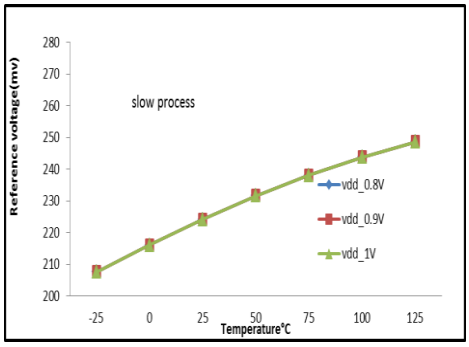
a. Slow process go to step 3.
b. Typical process go to step 5.
c. Fast process go to step 7.

3. If slow process then, read voltage and Temperature.
4. Return reference output voltage.
5. If typical process then, read voltage and Temperature.
6. Return reference output voltage.
7. If fast process then, read voltage and Temperature.
8. Return reference output voltage.
9. If Exit process then Exit.
10. End.

A) Slow Process Corner

Table 1 :(a) slow process corner

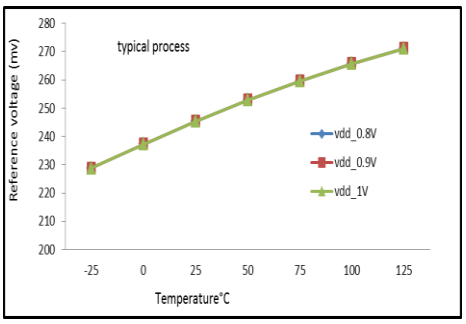
Temp in °C		-25	0	25	50	75	100	125
		Output voltage in mv						
Supply voltage in volt	vdd_0.8V	207.54	216.04	224.18	231.59	238.12	243.76	248.6
	vdd_0.9V	207.54	216.04	224.18	231.59	238.12	243.76	248.6
	vdd_1V	207.54	216.04	224.18	231.59	238.12	243.76	248.6



B) Typical Process Corner

Table 1 :(b) Typical process corner

Temp in °C		-25	0	25	50	75	100	125
		Output voltage in mv						
Supply voltage in volt	vdd_0.8V	228.8	237.24	245.35	252.85	259.64	265.71	271.1
	vdd_0.9V	228.8	237.24	245.35	252.85	259.64	265.71	271.1
	vdd_1V	228.8	237.24	245.35	252.85	259.64	265.71	271.1



C) Fast Process Corner

Table 1(c) Fast Process corner

Temp in °C		-25	0	25	50	75	100	125
		Output voltage in mv						
Supply voltage in volt	vdd_0.8V	251.137	258.5	266.34	274.23	281.88	289.07	295.7
	vdd_0.9V	251.13	258.5	266.34	274.236	281.88	289.07	295.7
	vdd_1V	251.13	258.5	266.34	274.23	281.88	289.07	295.7

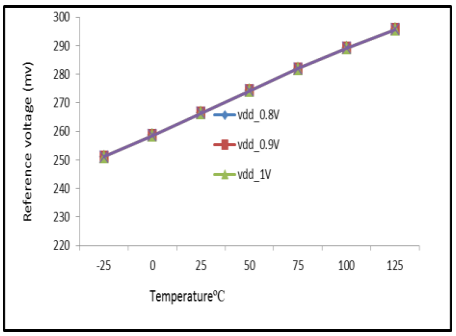


Fig.4.2.4. (d): Temperature dependence of reference voltage (Vout2) in different supply voltages and process corners.

The simulated results in different supply voltages and process corners with (L4/L3= 1.4) and temperature range of -25º C to 125 º C. As expected from (17), shows that the reference voltage (Vout2) increases linearly as temperature goes up. Also (Vout2) is not affected by the supply voltage and process corner.

2. Process Monitoring Circuit:

Algorithm:

1. Start
2. Read supply voltage and temperature.
3. Slow process corner.

Check output for voltage and Temperature.

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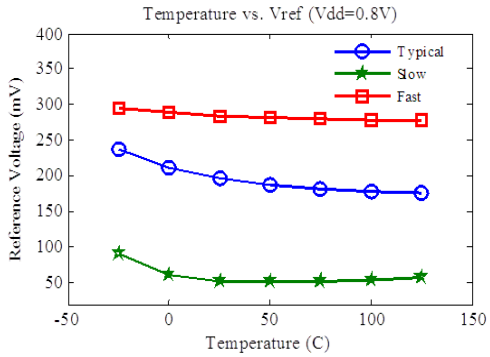
4. Typical process corner.
Check output for voltage and Temperature.
5. Fast process corner.
Check output for voltage and Temperature.
6. End.

A) SUPPLY VOLTAGE VDD= 0.8V

Table 2 (a) VDD = 0.8 V

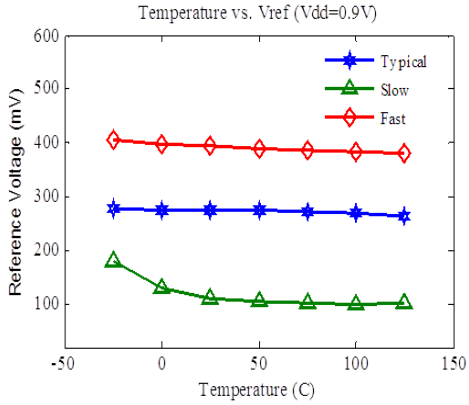
Vdd = 0.9V							
	Output voltage(mv)						
Temperature °C	-25	0	25	50	75	100	125
typical	237.39	212.75	197.24	188	182.64	179.366	177.14
Slow	90.68	61.762	58.039	55..65	53.21	52.79	51.65
Fast	294.87	288.82	284.78	281.82	279.73	278.61	278.74



B) SUPPLY VOLTAGE VDD= 0.9V

Table 2 (b) VDD = 0.9 V.

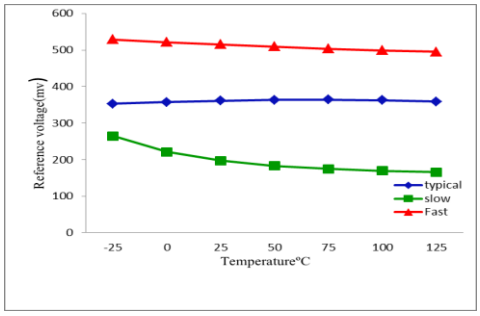
Vdd = 0.9V							
	Output voltage(mv)						
Temperature °C	-25	0	25	50	75	100	125
typical	276.95	275.29	274.88	273.97	271.96	268.89	264.91
slow	181.21	130.1	111.21	103.88	101.2	100.742	101.43
Fast	405.34	399.22	394.102	389.63	385.81	382.82	380.885



C) SUPPLY VOLTAGE VDD= 1.0V

Table 2 (c) VDD = 1.0V.

Vdd = 1V							
	Output voltage(mv)						
Temperature °C	-25	0	25	50	75	100	125
typical	353.26	357.33	361.22	363.77	364.31	362.64	358.85
slow	264.44	221.01	197.1	183.33	174.86	169.49	165.97
Fast	529.07	521.8	515.2	509.13	503.651	498.898	494.98



The simulated result shows the linear variation of the reference voltage according to process corner conditions. The reference voltage is not affected by temperature and supply voltage Variations.

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3. A/D Converter Circuit:

Algorithm:

1. Start
2. Read input voltage, clock and flag.
3. Invert input.
4. Return inverted output to flip flop.
5. Give output of D- flip flop to XOR gate.
6. Return Y1, Y2 and Y3 XOR gate output voltage.
7. If Y1Y2Y3 = "100"then
   Display low temperature or slow process corner.
8. If Y1Y2Y3 = "010"then
   Display medium temperature or typical process corner.
9. If Y1Y2Y3 = "001"then
   Display high temperature or fast process corner.
10. End.

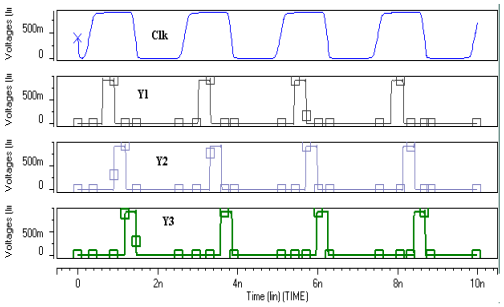

Fig.4.4.2: Three output-cases of the time-based A/D converter.

Fig.4.4.2 illustrates the XOR gate outputs for the 4-stage delay line The A/D converter has three cases:

1. Case #1Y1Y2Y3 = "100" is a low temperature or a slow process corner,
2. Case #2 Y1Y2Y3 = "010" is a medium temperature or a typical process corner, and
3. Case#3Y1Y2Y3 = "001" is a high temperature or a fast process corner.

4. Look Up Table:

Algorithm:

1. Start.
2. Read temperature T1T2T3 and process P1P2P3.
3. If ((T1T2T3 = "100") OR ((T1T2T3 = "010") OR ((T1T2T3 = "001")AND (P1P2P3 ="100"))
   Then display output.
4. If ((T1T2T3 = "100") OR ((T1T2T3 = "010") OR ((T1T2T3 = "001") AND (P1P2P3 ="010"))
   Then display output.
5. If ((T1T2T3 = "100") OR ((T1T2T3 = "010") OR ((T1T2T3 = "001") AND (P1P2P3 ="001"))
   Then display output.
6. End.

Table3
Measured Look up Table

Temperature °C			Process			Minimum Supply Voltage for Data Retention	Voltage level
-25	50	**125**	**S**	T	F		
1	0	0	1	0	0	0.66V	V1
0	1	0	1	0	0	0.63 V	V2
0	0	1	1	0	0	0.54 V	
1	0	0	0	1	0	0.59 V	V3
0	1	0	0	1	0	0.560 V	
0	0	1	0	1	0	0.480 V	V4
1	0	0	0	0	1	0.45 V	
0	1	0	0	0	1	0.42 V	V5
0	0	1	0	0	1	0.38 V	V6

5. Leakage Current Monitoring Circuit:

Algorithm:

1. Start.
2. Read temperatures and voltage.
3. Display leakage current components Isub and IBTBT.
4. End.

Table 4: Output of Leakage current Monitoring circuit for different values of Temperature

Temperature in °C	-25	0	25	50	75	100	125
Isub (nA)	1.19	2.3	4.14	6.94	10.93	16.31	23.26
I_{BTBT} (fA)	45.57	43.34	42.19	41.55	41.175	40.96	40.85

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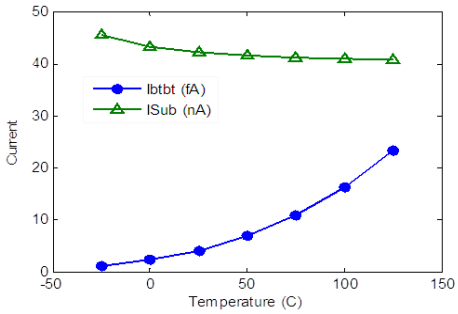

Fig.4.6.2: Leakage current as a function of temperature for leakage monitoring circuit

The simulated result shows that the subthreshold current (Isub) increases with increase in temperature and band to band tunneling current decreases with increase in temperature.

6. Current Comparator And Charge Pump Circuit:

Algorithm:

1. Start.
2. Read current and voltage.
3. If (Isub >IBTBT) then display charging of capacitor and increasing body bias voltage.
4. If (Isub =IBTBT) then display maintaining body bias voltage.
5. If (Isub <IBTBT) then display discharging of capacitor and decreasing body bias voltage.
6. End.

Table 5: Output of current comparator and Charge pump for different value of Isub and I_{BTBT}

Sr. No	Isub(nA)	I_{BTBT} (fA)	Modes of operation	Body bias voltage(Vbn)	Detection of Body bias voltage
1	6.94 (nA)	41.55 (fA)	Isub>Ibtbt	259.91 (mV)	Increasing the body-bias voltage.
2	41.55 (fA)	41.55 (fA)	Isub=Ibtbt	93.34mV	maintaining the body-bias voltage
3	6.94 (nA)	6.94 (nA)	Isub=Ibtbt	93.34mV	maintaining the body-bias voltage
4	41.55 (fA)	6.94 (nA)	Isub ? Ibtbt	12µV	decreasing the body-bias voltage

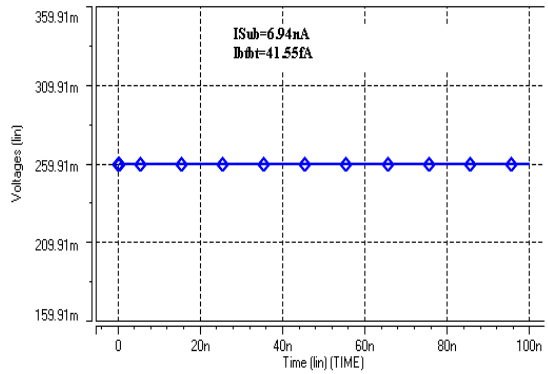

Fig.4.7.2 (a): Body Bias voltage for Isub > IBTBT

The simulated result shows that if Isub>IBTBT it charges the output capacitor of the charge pump, and increasing the body-bias voltage.

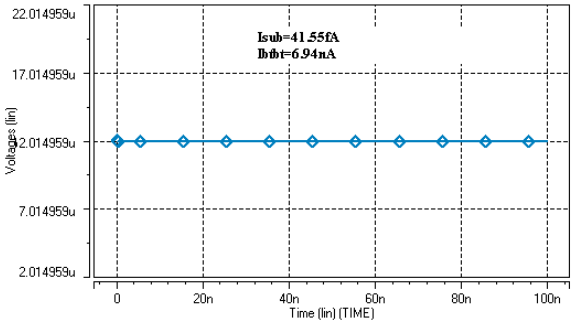

Fig.4.7.2 (b): Body Bias voltage for Isub < IBTBT

The simulated result shows that if Isub < IBTBT it discharges the output capacitor of the charge pump, and decreasing the body-bias voltage.

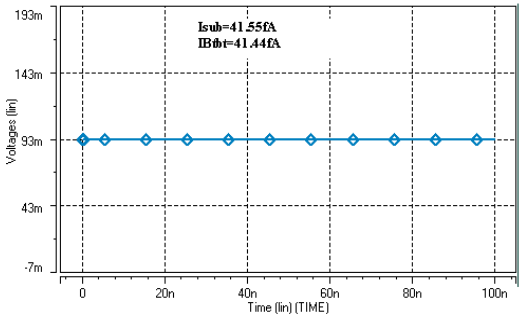

Fig.4.7.2 (c): Body Bias voltage for Isub = IBTBT

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The simulated result shows that if Isub=IBTBT, it maintains the body-bias voltage.

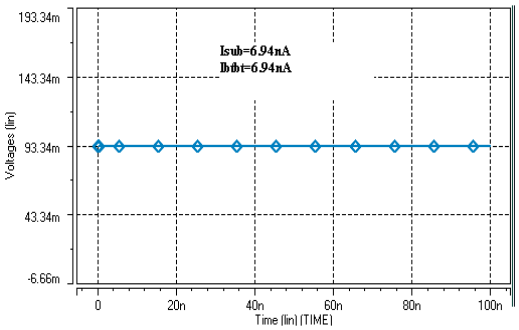

Fig.4.7.2 (d): Body Bias voltage for Isub = IBTBT

The simulated result shows that if Isub=IBTBT, it maintains the body-bias voltage.

V. CONCLUSION

As technology scales down below 90 nm, leakage currents have become a critical issue. In the past, circuit techniques and architectures ignored the effects of these currents because they were insignificant compared to the switching currents and threshold voltages were high enough. However, in modern technologies, the role of the leakage currents cannot be ignored and becomes increasingly significant issue with further scaling. Therefore, new circuit techniques and design considerations must be developed to control leakage currents in standby mode in order to provide low-power solutions.

In order to reduce standby power, this paper presents a novel control system that uses an adaptive method to find the optimal VDD/VBody scaling algorithm during standby mode. Based on the temperature and process conditions, the optimal supply voltages is generated to reduce the leakage power, and body-bias voltage is automatically adjusted continuously by the control loop to adapt to the PVT variations. By tuning body-bias voltage using leakage monitoring circuit, circuits can be biased at the optimal point where sub threshold-leakage current and BTBT leakage current are balanced to accomplish the minimum leakage power.

The results show that the proposed control system is a viable solution for high energy reduction in nanoscale CMOS circuits.

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