IJRDET
International Journal of Recent Development in Engineering and Technology
Website: www.ijrdet.com (ISSN 2347 – 6435(Online), Volume 1, Issue 1, Oct 2013)

Impact of Body Coefficient and Threshold Voltage on CNTFET with Varying Oxide Thickness

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***Abstract*— In this paper we analyze threshold voltage and body coefficient (ϒ) on varying the oxide thickness in CNTFET. Simulation analysis of drain current and drain voltage characteristic is discussed and found that due to decreasing nature of quantum capacitance in CNTFET, the factor (ϒ) has still impact on device and it is not negligible in deep nano regime. We also observed from simulation on nanohub, that the above mention characteristic is increasing while reducing the threshold voltage along with oxide thickness.**

Keywords-* *CNTFET, MOSFET, Quantum Capacitance, Threshold Voltage, Body Coefficient

I. INTRODUCTION

VLSI is characterized by the exponential growth of the number of transistor per chip. Gordon Moore noted that the number of transistor per chip wills double every 18 to 24 month [1]. Power delivery to the chip and thermal management are the challenges for high performance applications. As the performance is the main driver of technology development, ideal scaling rules have often been involved. However, leakage current shows a scaling behavior inverse to dynamic losses, so leakage power consumption is a new challenge which arises in the nanometer regime.

The exponential increase of leakage currents in a scaled device is an inevitable consequence of MOSFET physics. Unfortunately constant field scaling reaches a performance limit. This is due to some non scaling quantities that make an ideal constant field scaling impossible. Several circuit techniques to reduce the leakage power consumption have been proposed in literature. Even though the principle of these techniques is simple, the devil is in the implementation details. The first challenge is to determine whether a certain technique works in a particular technology. Field-effect transistors based on CNTs (carbon nanotubes) have been a focus of active research in recent years [2]-[6]. The device characteristics, such as transconductance and subthreshold swing, show an order of magnitude improvement with a CNT gate compared to the global back gate.

II. PHYSICS OF MOSFET

The most important field effect transistor is the MOSFET. In silicon MOSFET, the gate contact is separated from the channel by an insulating silicon dioxide layer. The charge carriers of the conducting channel constitute an inversion charge, that is, electrons in the case of n-channel device or holes in the case of p-channel device. The electrons enter and exit the channel at *n* + source and drain contacts in the case of an *n*-channel MOSFET, and at *p* + contacts in the case of a *p*-channel MOSFET. Beside the speed of a digital integrated circuit, the power dissipation has always been an important issue. A MOSFET consists of doped silicon substrate with two, highly doped contacts, source and drain. The so-called channel region in-between is covered by an insulating layer, the gate-oxide, which is in contact with the gate electrode. A MOSFET is based on the modulation of charge concentration by a MOS capacitance between a body electrode and a gate electrode located above the body and insulated from all other device regions by a gate dielectric layer which in the case of a MOSFET is an oxide, such as silicon dioxide. Without applying a voltage at the gate electrode, no current can flow from source to drain as the pn-juctions between each contact and the substrate act as two opposite diodes. When applying a voltage at the gate electrode, a channel is form close to the gate oxide and current can flow between source and drain.

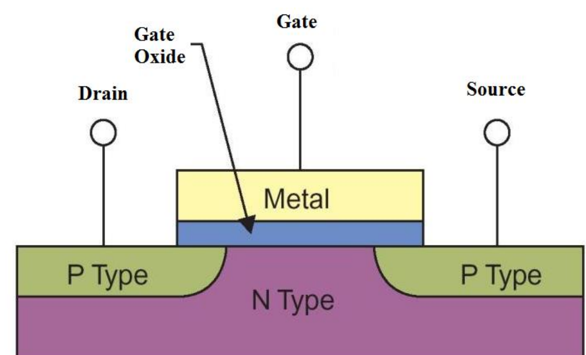

Fig. 1 Schematic of MOSFET device

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In the past several years, significant progress has been made for the scaling of MOSFET structure to gate lengths below 60nm. Further scaling of the structure becomes increasingly challenging due to excess leakage, degradation in mobility and a variety of difficulties within the device processing. At less than 1 nm thicknesses of oxide, the quantum mechanical tunnelling currents through the oxide become intolerable.

III. CNT AND CNTFET

A. *Carbon nanotube (CNT)*

Carbon nanotubes are allotropes of carbon. Allotropism is the property of some chemical element to exist in two or more different forms, known as allotropes of these elements. Carbon nanotubes are cylindrical carbon molecules with novel properties that make them potentially useful in a wide variety of applications in nano-electronics. Carbon nanotube (CNT) is a promising alternative to conventional silicon technology for future nanoelectronics because of their unique electrical properties. Carbon nanotubes are rolled up sheets of grapheme as shown in Fig.2. CNT is exceptional in that it has a perfect crystalline structure, which is composed of strong covalent C-C bonds.

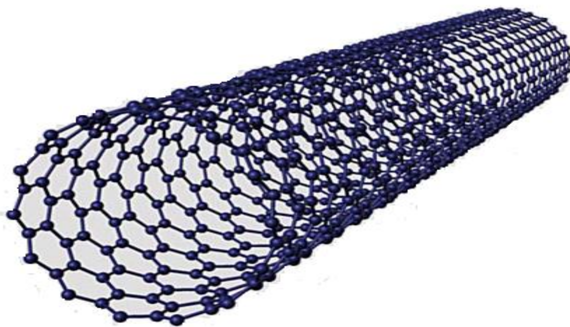

Fig. 2. CNT rolled to form CNTFET

CNTFET uses CNT as a channel between source and drain in conventional silicon MOSFET . It may be single waal nanotube (SWNT) or multi wall nanotube (MWNT), depending upon the no. of tubes used as a channel. Semiconducting SWNTs are of special interest because they are promising in producing semiconducting devices that rival devices made by traditional Si technology [7]-[10].

B. *CNTFET*

Carbon nanotube field effect transistor (CNTFET) refers to a field effect transistor that utilizes a single carbon nanotube or an array of carbon nanotubes as the channel material instead of bulk silicon in the traditional MOSFET structure. Carbon nanotubes are a new modification of carbon discovered in 1991 by S. Ijiima [11]. The undoped semiconducting nanotubes are placed under the gate as channel region, while heavily doped CNT segments are placed between the gate and the source/drain to allow for a low series resistance in the ON-state [12]. The gate-to-source voltage that generates the same reference current is taken as the threshold voltage for the transistor that has different chirality. CNTFETs provide a unique opportunity to control threshold voltage by changing the chirality vector, or the diameter of the CNT [13].

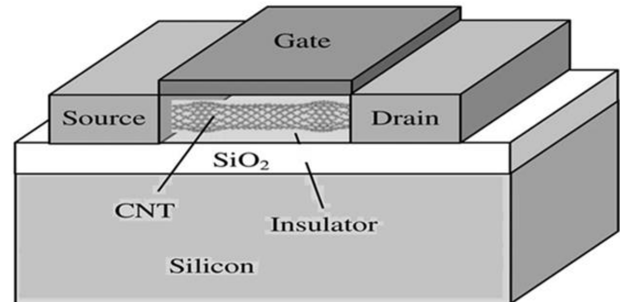

Fig.3. Cross-sectional view of Carbon nanotune FET

The I–V characteristics of the CNTFET are similar to MOSFET. The threshold voltage is defined as the voltage required to turn-on the transistor. The threshold voltage of the intrinsic CNT channel can be approximated to be of first order as the half band-gap is an inverse function of the diameter [14]. Similar to the traditional silicon device, the CNTFET also has four terminals.

IV. IMPACT OF THRESHOLD VOLTAGE

With ongoing technology scaling, leakage power gains more and more importance. In low power systems with low activity profile, the standby power is often more important than the dynamic power consumption. Hence, slack can be used primarily to reduce leakage currents by using devices with an increased threshold voltage for the gates in subcritical paths. A higher threshold voltage is used for leakage optimization in less performance circuits, and the low threshold voltage is used to the most performance critical circuits.

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In summary, the use of an increased threshold voltage in sub critical paths is beneficial to suppress sub threshold leakage. However, the amount of the gates with the low threshold devices must be small compared to the high threshold gates in order to achieve a significant leakage reduction of the overall system. The use of an increased threshold voltage to reduce the leakage power consumption of subcritical paths must be done under the strict consideration of threshold and supply voltage variations. According to the alpha power delay model (Eq.1), the delay of a cmos gate would become infinite when the threshold and supply voltage converge. The delay with respect to the supply and the threshold voltage is given by:

$$t_d = \frac{V_{DD}}{(V_{DD}-V_{th})^{\alpha}} \qquad \text{--- Eq. 1}$$

The sensitivity of the delay on threshold and supply voltage variations increases with increasing threshold and decreasing supply voltage. The delay variation becomes huge for high threshold and low supply voltages. With decreasing supply voltage and increasing threshold voltage, the gate delay becomes more sensitive on voltage variations.

The power versus delay design space is mainly dominated by the threshold voltage and the supply voltage. To cope with various performance requirements, it would be beneficial if the threshold voltage was an independent and tunable design parameter. A negative bulk to source voltage for a MOS transistor increase the width of the bulk depletion layer and increase the threshold voltage. The shift of the MOS threshold voltage due to the change in the bulk-to-source voltage is given by Eq.2.

$$\Delta V_{th} = \Upsilon\left(\sqrt{(|2\psi_B - V_{BS}|)} - \sqrt{|2\psi_B|}\right) \qquad \text{---Eq.2}$$

$$\Upsilon = \frac{\sqrt{2q\,\epsilon_{Si} N_B}}{C_{ox}} \qquad \text{---Eq.3}$$

$$C_{ox} = \frac{\epsilon k A}{T_{ox}} \qquad \text{-----Eq.4}$$

Where Υ is the body coefficient and is the barrier potential. As shown in Eq.3 body coefficient is inversely proportional to oxide capacitance and oxide thickness is also inversely proportional to (Eq.4). In nanometer regime when oxide thickness goes on decreasing quantum capacitance will increase and subsequently body coefficient will decrease and it is negligible.

But in the case of CNTFET as the oxide thickness goes on decreasing the quantum capacitance will also increased at gate voltage 0.5 V and above, which is shown in Fig. 4.

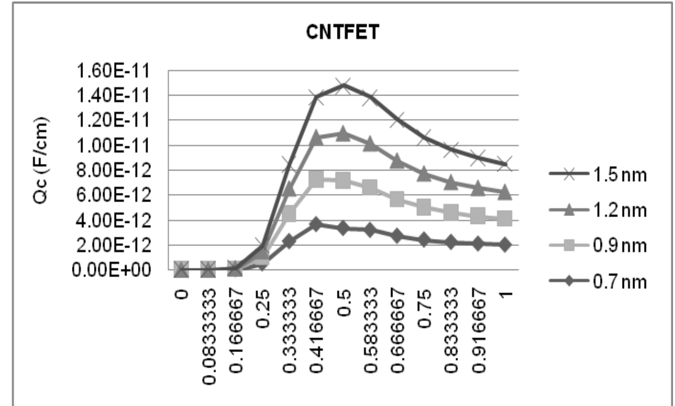

Fig.4. Plot of Quantum Capacitance Vs. gate Voltage for different oxide thickness

V. Simulation Analysis

Simulation of drain current vs. drain voltage characteristic for different oxide thickness is done through online simulator of nanohub.org. For simulation there are 13 different drain voltages are consider with step voltage of 0.083V between 0 and 1 V. As far as oxide thickness is concerned five different oxide thicknesses such as 1.5 nm, 1.2 nm, 0.9 nm, 0.7 nm, and 0.5 nm. are considered. Result shown in Fig.5, shows that while reducing the oxide thickness from 1.5 nm to 0.5 nm, the drain current vs. drain voltage characteristic goes on increasing at fixed gate voltage of 1 V and threshold voltage 0.25 V.

As the gate voltage reduces from 1 V to 0.75 V the characteristic of drain current with respect to drain voltage decreases while reducing the oxide thickness compare to the previous condition at gate voltage of 1 V, which is shown in the plot of Fig.6. Simulation result shown in Fig.7 and Fig.8 indicates that the same characteristics as we have dissused above, the only difference is that in these two simulation we have considered threshold voltage 0.32 instead of 0.25 V.

VI. Conclusion

Drain current with respect to drain voltage is important characteristic in any device. In this paper we analyze the simulation for different oxide thickness of CNTFET in nanohub and concluded that in nanometer regime threshold voltage and body coefficient has important role.

In MOSFET body coefficient parameter is negligible small in sub- nanometer regime but in case of CNTFET it is not negligible as the quantum capacitance goes on decreasing after 0.5 V and above gate voltage which results reduced oxide capacitance and finally some value of body coefficient (Υ).

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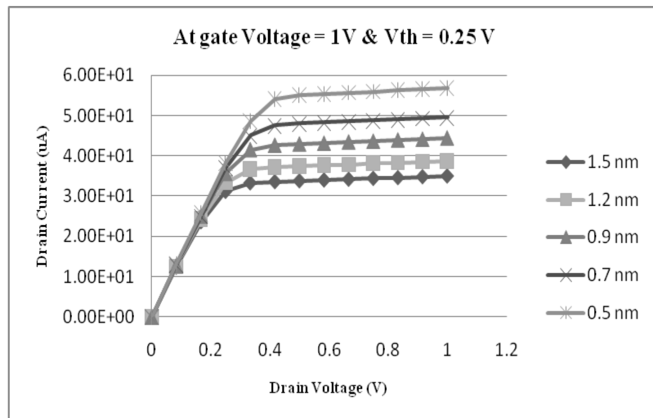

Fig.5. Drain current Vs. Drain voltage of CNTFET at gate voltage 1 V and Vth 0.25V for different Oxide thickness.

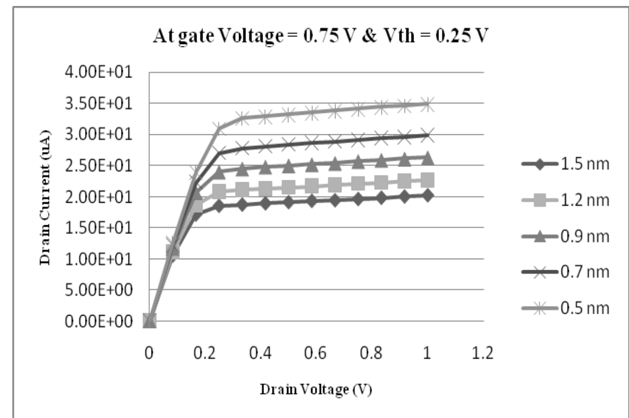

Fig.6. Drain current Vs. Drain voltage of CNTFET at gate voltage 0.75 V and Vth 0.25V for different Oxide thickness.

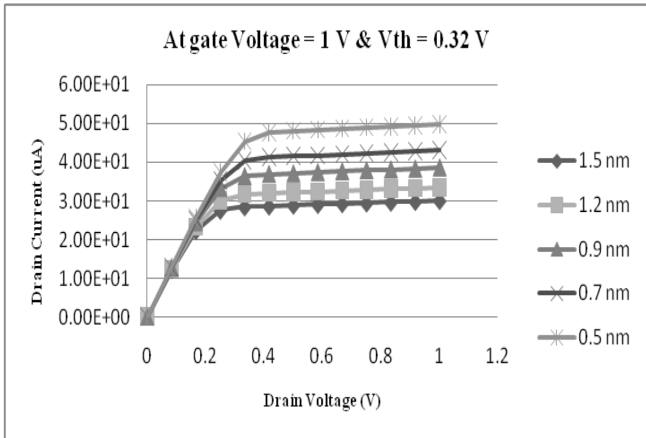

Fig.7. Drain current Vs. Drain voltage of CNTFET at gate V and Vth 0.32V for different Oxide thickness.

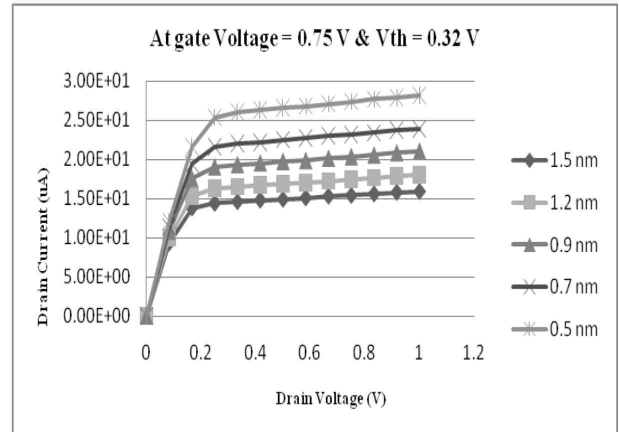

Fig. 8. Drain current Vs. Drain voltage of CNTFET at gate voltage 1 voltage 0.75 V and Vth 0.32V for different Oxide thickness.