International Journal of Recent Development in Engineering and Technology
Website: www.ijrdet.com (ISSN 2347 – 6435(Online), Volume 1, Issue 1, Oct 2013)

Optimization of Direct Tunneling Gate Leakage Current in Ultrathin Gate Oxide FET with High-K Dielectrics

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***Abstract*-- This paper presents the impact of parameter optimization of n-type MOSFET for direct tunneling gate current using ultrathin Si3N4 and HfO2 with EOT (Equivalent Oxide Thickness) of 1.0 nm. This work is compared with TCAD santaurus simulation results to verify that accuracy of the model and excellent reduction in gate leakage with the introduction of the high-k gate dielectrics (HfO2 & Si3N4) in place of SiO2. It also observed that high-k based MOSFET exhibits improved performance of Subthreshold Swing, I_{on}, I_{off} I_{on}/I_{off} ratio and transconductance.**

I. INTRODUCTION

The great advantage of MOS technology is the scaling. The reduction of the dimensions of a MOSFET has been dramatic during the last four decades. In scaling down the lateral dimension of the MOSFETs, such as L & W, it is necessary to decrease the oxide thickness and increase the channel doping, so as to maintain the electrostatic integrity [1, 2]. Constant field theory requires that gate oxide thickness should scale to minimum Length & Width. Aggressive scaling in recent years has reduced oxide (SiO_2) gate dielectric thickness. The reduction of the dielectric thickness (SiO_2) in the subnanometric range produces dramatic gate leakage issues detrimental for the performance [1].The excellent dielectric properties of silicon dioxide (SiO_2) have aided the evolution of microelectronics during the past decades. Reduced feature size improves the performance of an integrated circuit. However the performance of SiO2 as dielectric sets a limit on device scaling. In metal oxide field effect transistor (MOSFET) dielectric films with higher dielectric constant have better control over the channel electrons. A number of high dielectric materials are available to replace SiO_2, but most of them have inherent disadvantages and incompatible with existing fabrication technology. Hafnium based oxides have shown encouraging performance as high-k dielectric in submicron device[3].The introduction of high-κ materials (or high-dielectric permittivity material) enables to keep increasing the inversion charge density without reducing the physical dielectric thickness. The physical thickness has been replaced by an electrical thickness or Equivalent Oxide Thickness (EOT). EOT scaling improves the devices performance through the inversion charge density increase with a reasonable level of gate leakage.

In this work, we have presented direct tunneling leakage current through ultrathin HfO_2 and Si_3N_4 gate dielectrics in n-type MOSFET using TCAD Simulation.

1.1 Gate Leakage:

As the continuous down-scaling of the device size has lead to very thin gate oxides, the leakage current that can flow from the channel to the gate comes into the order of the subthreshold leakage current and the gate cannot be considered as an ideally insulated electrode anymore. This affects the circuit functionality and increases the standby power consumption due to the static gate current. For dynamic logic concepts the gate leakage drastically reduces the maximum clock cycle time [4]. Two tunneling mechanisms are responsible for the gate leakage, Fowler-Nordheim tunneling and direct tunneling [5]. The gate leakage increases exponentially as the oxide thickness is reduced. This limits the downscaling of the oxide thickness to about 1.5-2 nm when looking at the total standby power consumption of a chip [6]. To further decrease the effective oxide thickness alternative high dielectric constant materials can be used [7]. On the other hand, a thin gate oxide reduces the short-channel effect and improves the driving capabilities of a MOS transistor. However, a tradeoff between this benefit and the gate leakage is necessary.

1.2 Direct Tunneling

The phenomenon of tunneling, which has no counterpart in classical physics, is an important consequence of quantum mechanics [8]. It is the quantum mechanical effect of transitioning through a classically-forbidden energy state. In current microelectronic devices, tunneling has become a very important physical effect. In some devices, tunneling leads to undesired leakage currents (for gates in small MOSFETs). For other devices such as EEPROMs, tunneling is essential for the operation of the device. Tunneling also plays a role in some generation–recombination models. There are three ways of model the gate leakage in which the direct tunneling is the powerful model. This model describes leakage through thin gate insulators, provided those are of uniform or of uniformly graded composition. This model :i) Assumes a trapezoidal barrier (this restricts the range of application to tunneling through insulators). ii) Neglects heating of the tunneling carriers.iii) optionally, accounts for image charge effects (at the cost of reduced numeric robustness) [9].

The electron tunneling density used by the tunneling model is given by [5].

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$$j_n = \frac{qm_c k}{2\pi^2\hbar^3}\int_0^\infty dEY(E)\left\{T(0)\ln\left(\exp\left[\frac{E_{F,n}(0)-E_c(0)-E}{kT(0)}\right]+1\right) - T(d)\ln\left(\exp\left[\frac{E_{F,n}(d)-E_c(0)-E}{kT(d)}\right]+1\right)\right\}$$

Where d is the effective thickness of the barrier, mc is a mass prefactor, the argument 0 denoted one (the "substrate) side of the barrier and d denotes the other ('gate') side, and E is the energy of the elastic tunnel process(relative to $E_c(0)$.

$\Upsilon(E) = 2/(1+g(E))$ is the transmission coefficient for the trapezoidal potential barrier, with:

$$g(E) = \frac{\pi^2}{2}\left\{\sqrt{\frac{E_T}{E}}\sqrt{\frac{m_{Si}}{m_G}}\left(Bi_d'Ai_0 - Ai_d'Bi_0\right)^2 + \sqrt{\frac{E}{E_T}}\sqrt{\frac{m_G}{m_{Si}}}\left(Bi_dAi_0' - Ai_dBi_0'\right)^2 + \frac{\sqrt{m_G m_{Si}}}{m_{ox}}\frac{\hbar\Theta_{ox}}{\sqrt{EE_T}}\left(Bi_d'Ai_0' - Ai_d'Bi_0'\right)^2 + \frac{m_{ox}}{\sqrt{m_G m_{Si}}}\frac{\sqrt{EE_T}}{\hbar\Theta_{ox}}\left(Bi_dAi_0 - Ai_dBi_0\right)\right\}$$

and:

$$Ai_0 = A_i\left(\frac{E_B(E)-E}{\hbar\Theta_{ox}}\right), \quad Ai_d = A_i\left(\frac{E_B(E)-qF_{ox}d-E}{\hbar\Theta_{ox}}\right)$$

and so on, where $\hbar\Theta_{ox} = (q^2\hbar^2F_{ox}^2/2m_{ox})^{1/3}$ and $E_B(E)$ denotes the (substrate-side)barrier height for the electrons of energy E. E_T is the tunneling energy with respect to the conduction band edge on the gate side, $E_T = E - E_c(d) - E_c(0)$.

$F_{ox} = V_{ox}/d$ is the electric field in the oxide. The quantities m_G, m_{Si} & m_{ox} represents the electrons masses in the three materials, respectively. Ai and Bi are the Airy functions and Ai' & Bi' are their derivatives. Here we are ignoring the image-force effect.

1.3 High-K Dielectrics

The term **high-κ dielectric** refers to a material with a high dielectric constant κ (as compared to silicon dioxide). High-κ dielectrics are used in semiconductor manufacturing processes where they are usually used to replace a silicon dioxide gate dielectric or another dielectric layer of a device. The implementation of high-κ gate dielectrics is one of several strategies developed to allow further miniaturization of microelectronic components, colloquially referred to as extending Moore's Law [10].

Tunneling currents decrease exponentially with increasing distance. An FET is capacitance-operated device, where the source-drain current of the FET depends on the gate capacitance,

$$C = \varepsilon_0 KA/t$$

Where ε_0 is the permittivity of free space , K is the relative permittivity, A is the area and t is the SiO_2 thickness. Hence, the solution to the tunneling problem is to replace SiO_2 with a physically thicker layer of a new material of the high dielectric constant(permittivity) K, Fig.1.This will keep the same capacitance, but will decrease the tunneling current. These new gate oxides are called 'high k oxides' [11].

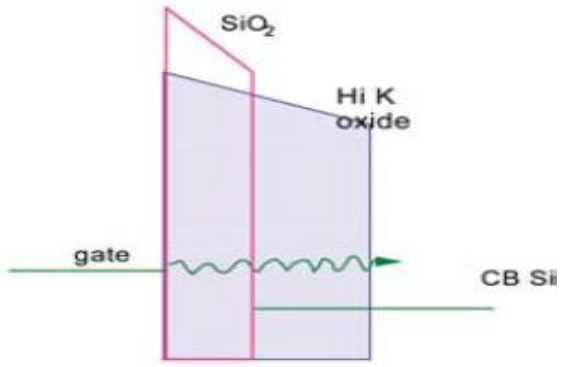

Fig.1. Schematic of Direct Tunneling through SiO2 layer and High-K Dielectrics.

HfO_2 has been extensively studied due to its high dielectric constant and large energy band gap with high band offset.

1.3.1 Challenges with High-k Dielectric

High-k dielectric gate oxide faces several challenges in MOS-devices. The major concerns are structural defects, mobility degradation, interface fixed charge, and dopant depletion in the poly-Si gate electrode.

i) Structural Defects

The high-k gate dielectric has higher defect concentration than SiO_2. In SiO_2 defects are mainly due to dangling bond and low coordination. Dangling bond can be removed by re-bonding the network especially at the Si/SiO_2 interface. On the other hand the high-k bonding structure is ionic and coordination number is higher [12]. Therefore high-k dielectric is poor glass formers and it has high defect concentration.

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ii) Mobility Degradation

The degradation of carrier mobility in the channel is another major concern. The mobility of high-k dielectric oxides is lower than that of SiO_2 due to the interface roughness over range of interest.

iii) Threshold Voltage Control

The high-k dielectric material shifts the flat band voltage which changes the threshold voltage of the device. Large defect density of high-k dielectric oxides results VFB 0.5-1V [12].

iv) Gate Electrode Selection

The gate electrode selection is a challenge in high speed sub micron MOSFET .Poly-Si gate can be formed by ion implantation and subsequently annealing.

1.3.2 Desirable Criteria of High-k Dielectric

With the scaling of the MOS-device ultra-thin SiO_2 suffers some unsolvable issues. Therefore, it is necessary to replace the SiO_2 with a thicker layer of higher dielectric constant. Since high-k dielectric is not as favourable as the native oxide (SiO2) some factors need to be considered while replacing SiO_2 by other dielectric materials

1.3.2.1 Equivalent Oxide thickness (EOT)

Equivalent oxide thickness is defined as thickness of SiO_2 layer that would be required to achieve the same capacitance as the high-k material in consideration. It is defined as [13]

$$EOT = t_{high-k}\left(\frac{K_{SiO_2}}{K_{high-k}}\right)$$

A suitable alternative high-k gate dielectric has to be found to meet the equivalent oxide thickness required by ITRS.

1.3.2.2 Energy Band Gap

The band gap of the high-k material decreases with the increase of the permittivity which is given by

$$E_G = 20\left[\frac{3}{(2+\epsilon)}\right]^2$$

1.3.2.3 Thermodynamic Stability

The interface between ultra thin gate dielectric with Si plays a key role in determining the electrical properties of MOSFETs.

II. PHYSICS & STRUCTURE OF THE MOSFET

The device structure of the N-MOSFET with high-k dielectrics used in this simulation study is shown in fig. 3

The embedded Si-source is heavily doped with $10^{20}\,cm^{-3}$ n-type, the body region is doped p-type with $10^{20}\,cm^{-3}$, and the Si drain region is also doped n-type $10^{19}\,cm^{-3}$. This device has a 50-nm-thick N+ poly-Si gate with metallurgical gate length of 25nm with V_T of 0.19V. The EOT has been taken as 1.0 nm. The upper part of the polySi gate is doped with $10^{22}\,cm^{-3}$ and lower part is doped with$10^{20}\,cm^{-3}$. The oxide spacer has been assumed to reduce the gate capacitance. The overlap length L_{ov}(5nm) is controlled by the source and drain implantation energy.

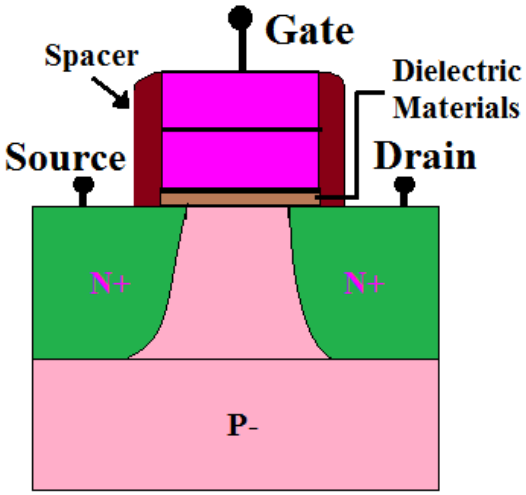

Fig.2. Device structure of the N-MOSFET with high-k dielectric.

The parameters used for the simulation of the given MOSFET are mentioned in Table I. [14, 15] as shown below.

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TABLE I
PARAMETERS USED FOR MOSFET DEVICE

Parameters	This Work		
	SiO_2 ECB	Si_3N_4 ECB	HfO_2 ECB
Tunneling Barrier Height($\emptyset_{ox}$)	3.15 (eV)	2.10 (eV)	1.7 (eV)
Tunneling Effective Mass(m_{ox})	$0.5m_o$	$0.40m_o$	$0.20m_o$
Dielectric Constant(k)	3.9	7.5	22
Fitting Parameter(α)	0.88	0.80	0.68

III. RESULT

This section shows the TCAD simulation of NMOSFET, in which the gate leakage current is reduced by the replacement of gate oxide with the High-K dielectric (Si_3N_4, HfO_2).

Fig.3 shows the simulation if the gate tunneling current of the n-type MOSFET with different high-k dielectrics structures has been carried out.

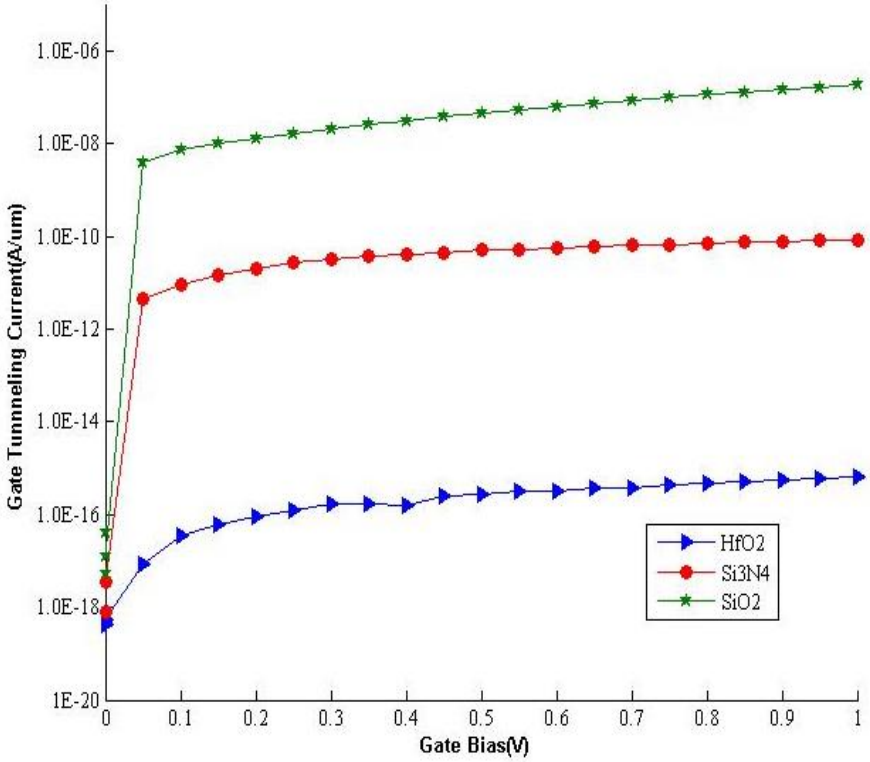

Fig.3. Gate Tunneling Current Vs Gate Bias for different high-k dielectrics.

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Fig.4 plots the drain current Vs gate voltage of the device which shows the variation of drain current with gate voltage using different high-k dielectrics. This improvement in drain current is due to the reduction in threshold voltage which is shown in fig.5

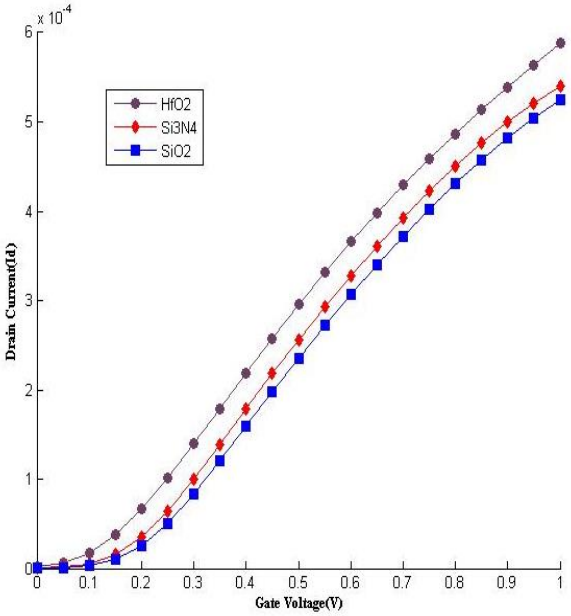

Fig.4. Gate Tunneling Current Vs Gate Bias for different high-k dielectrics.

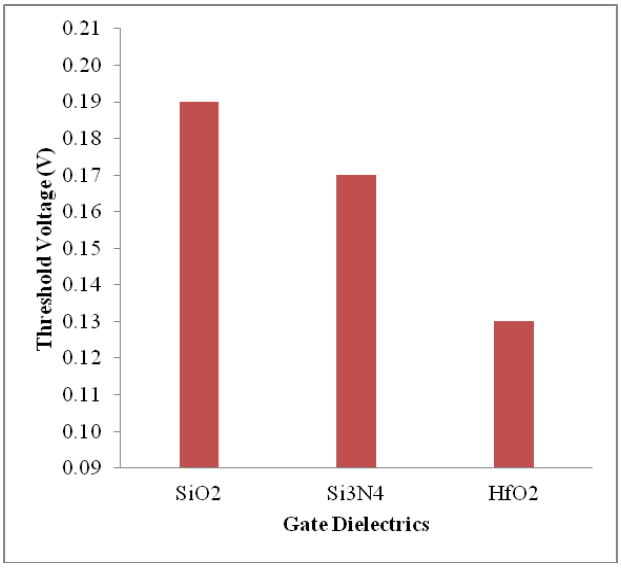

Fig.5. Threshold (V_T) Vs Gate Dielctric Materials.

Fig.6 shows that the transconductance enhancement by using different high-k gate dielectric materials.

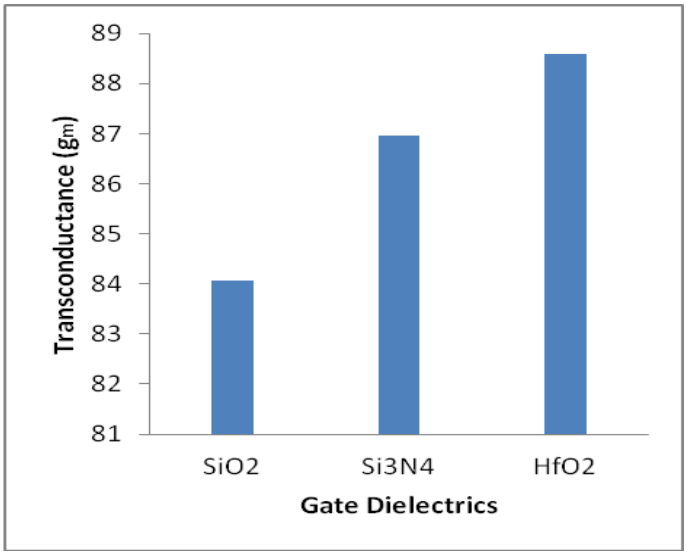

Fig.6. Transcondutance (g_m) Vs Gate Dielctric Materials

Fig 7. shows the on current variation with different dielectric material of the device to show the effect of the dielctric material.HfO_2 based device shows the good Ion current in comaprision to other two dielectric materails SiO_2 and Si_3N_4.

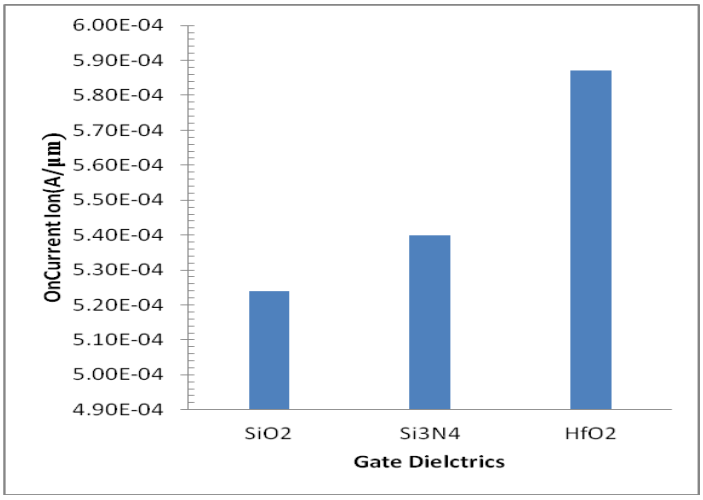

Fig.7. On Current (Ion) Vs Gate Dielctric Materials.

Fig. 8 shows the effect of high-k dielectrics on off current of the device. The subthreshold voltage decreases with increase in fringing field coupling with channel carrier, so, so the introduction of the high-k increases the off current of the device.

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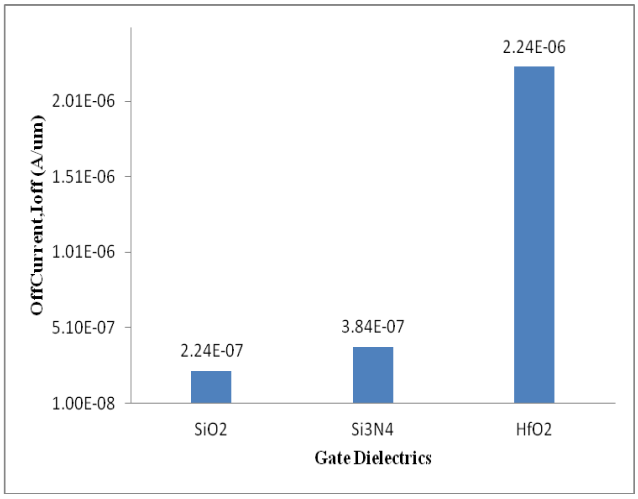

Fig.8. On Current (Ion) Vs Gate Dielctric Materials.

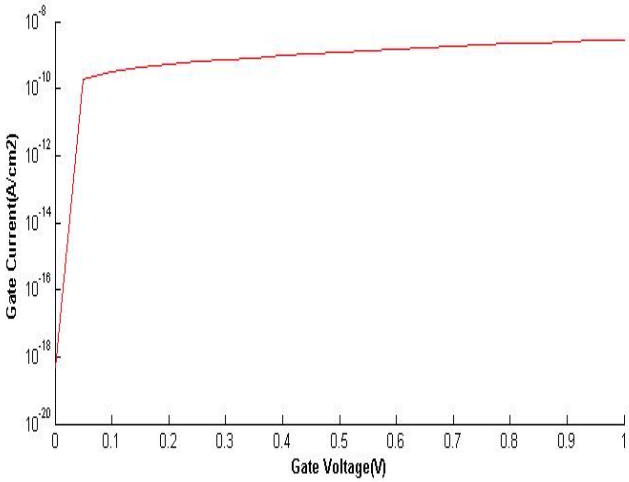

Fig.9. Gate current density Vs Gate Voltage of NMOSFET for SiO2

Fig.9 and Fig.10 shows the gate tunneling current with gate voltage for the SiO2 gate dielectrics in NMOSFET and PMOSFET. From both plots we can see that the tunneling current through SiO2 is considerably lower in the P^+ poly-Si PMOSFET than in N^+ poly-Si NMOSFET. The reason is the barrier height for PMOSFET being significantly higher than that for NMOSFET in case of SiO2 gate dielectric.

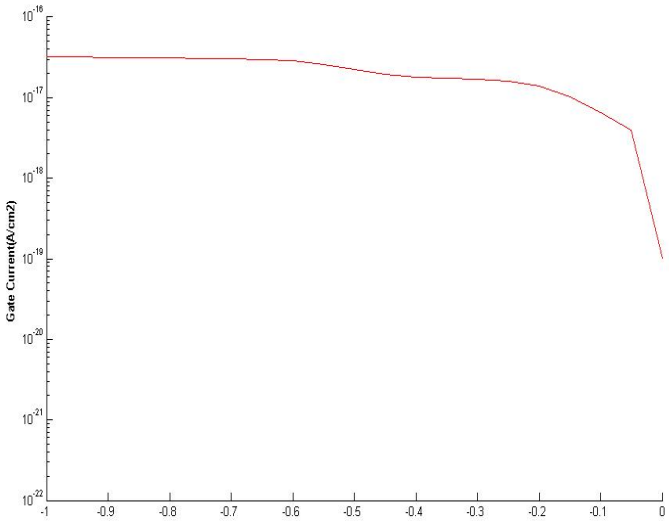

Fig.10. Gate current density Vs Gate Voltage of PMOSFET for SiO2

IV. CONCLUSION

With the increasing importance of the tunneling currents, a good qualitative understanding of direct tunneling currents is essential. Gate leakage reduction is the key motivation for the replacement of SiO_2 with alternative gate dielectrics. In this work, we studied the optimization of the N-type MOSFET for direct tunneling gate current using ultrathin Si_3N_4 and HfO_2 with EOT (Equivalent Oxide Thickness). TACAD simulation is used to verify the accuracy and excellent reduction in gate leakage of the model using dielectrics Si_3N_4 and HfO_2.It also observed that high-k based MOSFET exhibits improved performance of sub threshold swing and transconductance and on current.

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