International Journal of Recent Development in Engineering and Technology
Website: www.ijrdet.com (ISSN 2347-6435 (Online) Volume 15, Issue 06, June 2026)

Artificial Intelligence Assisted Digital VLSI Design: With a Review of Past Research and Emerging Trends

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***Abstract*—. The rapid advancement of semiconductor technology has significantly increased the complexity of digital Very Large Scale Integration (VLSI) systems. Traditional VLSI design methodologies face challenges related to power consumption, design complexity, verification time, and manufacturing constraints. Recent developments in Artificial Intelligence (AI) and Machine Learning (ML) have introduced innovative solutions for automating and optimizing various stages of the VLSI design flow. This paper presents a comprehensive review of the evolution of digital VLSI design and examines the impact of AI-driven techniques on chip design, floor planning, routing, power optimization, verification, and manufacturing. The study highlights how AI is transforming conventional Electronic Design Automation (EDA) tools and discusses future research opportunities in autonomous chip design.**

***Keywords*—Digital VLSI, Artificial Intelligence, Machine Learning, EDA, Floor planning, Routing, Power Optimization, System-on-Chip.**

I. Introduction

Digital VLSI design is the process of integrating millions or billions of transistors onto a single semiconductor chip to implement complex digital systems. The evolution of VLSI technology has enabled the development of high-performance processors, embedded systems, mobile devices, and artificial intelligence accelerators.[1]

Historically, VLSI design relied heavily on manual optimization and rule-based Computer-Aided Design (CAD) tools. As technology nodes continued to shrink below 10 nm, design complexity increased dramatically, creating challenges in timing closure, power management, verification, and physical design. Artificial Intelligence has emerged as a promising solution to address these challenges by enabling data-driven optimization and automation throughout the VLSI design process.

II. Literature Review

A. Early research focused on CMOS scaling, transistor optimization, and structured design methodologies. The introduction of Hardware Description Languages (HDLs) such as Verilog and VHDL improved design productivity and abstraction.

Major research areas included:

- Logic synthesis
- Physical design automation
- Timing optimization
- Low-power design techniques
- System-on-Chip integration

B. Low-Power VLSI Research

Power consumption became a critical concern with the growth of portable electronics.

Researchers introduced:

- Clock gating
- Power gating
- Dynamic Voltage and Frequency Scaling (DVFS)
- Multi-threshold CMOS technology

These methods reduced both dynamic and static power consumption while maintaining performance requirements.

C. AI in Electronic Design Automation

Recent studies have explored the integration of Machine Learning algorithms into Electronic Design Automation tools. AI techniques enable prediction, optimization, and automation of complex design decisions that traditionally required extensive human expertise. Figure below shows design flow figure 1.1[8].

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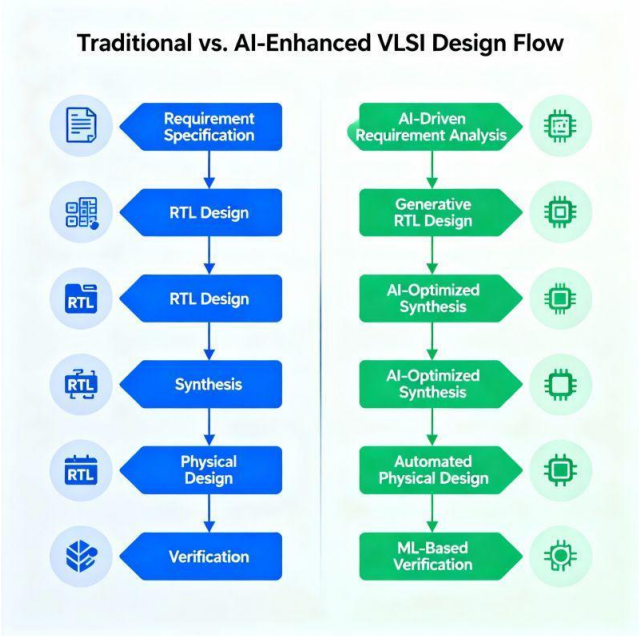

Figure 1.1

III. Research Challenges In Modern VLSI Design

The semiconductor industry currently faces several challenges:

1) Design Complexity

Modern System-on-Chip designs contain billions of transistors and thousands of interconnected modules.

2) Power Consumption

Increased transistor density leads to higher power dissipation and thermal management issues.

3) Verification Bottleneck

Verification can consume more than 60% of the total design cycle.

4) Routing Congestion

Advanced technology nodes require complex interconnect structures that significantly affect timing and area.

5) Manufacturing Variations

Process variations can impact yield, reliability, and overall chip performance.

IV. Artificial Intelligence in Digital VLSI Design

A. AI-Based Floor planning

Floor planning determines the physical placement of major functional blocks within a chip.

Machine Learning algorithms analyze previous designs and predict optimal block placement to minimize:

- Wire length
- Congestion
- Power consumption
- Timing violations

Benefits include reduced design iteration time and improved layout quality. Floor planning demonstrate by Figure1.2[9].

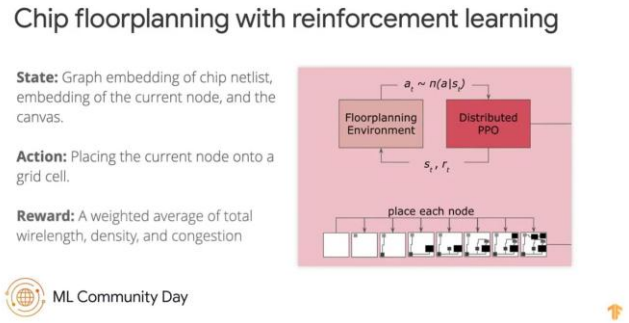

Figure 1.2

B. AI-Assisted Placement and Routing

Routing is one of the most computationally intensive stages of physical design.

Deep Learning and Reinforcement Learning models are used to:

- Predict congestion hotspots
- Optimize routing paths
- Minimize delay
- Reduce interconnect power

AI-assisted routing improves design quality while reducing computational overhead. This is shown below in Figure1.3[10][11].

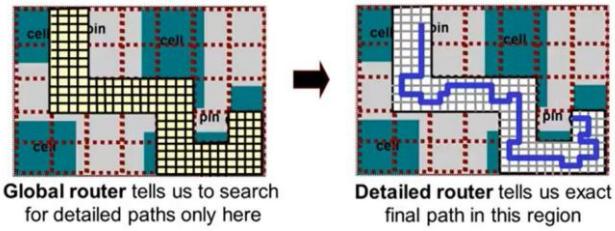

Figure 1.3

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C. Machine Learning for Power Optimization

Machine Learning models estimate power consumption based on switching activity and circuit characteristics.

Applications include:

- Dynamic power prediction
- Leakage current estimation
- Thermal-aware optimization
- Adaptive voltage scaling

These techniques improve energy efficiency in modern integrated circuits.

D. AI-Driven Verification and Testing

Functional verification is a major contributor to design cost and development time.

AI methods assist in:

- Automatic test pattern generation
- Defect prediction
- Bug localization
- Coverage optimization

Machine Learning enables faster fault detection and improved verification efficiency. It is demonstrated in figure 1.4[11][12]

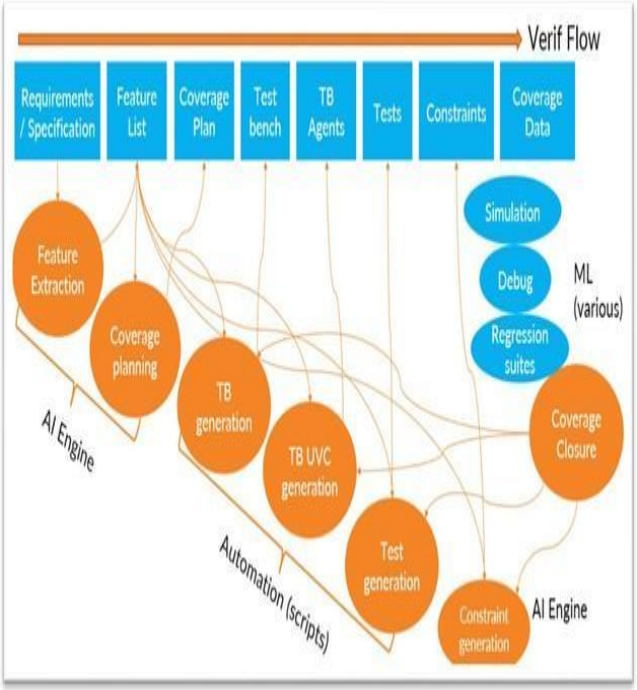

Figure 1.4

E. Yield Prediction and Process Optimization

Manufacturing defects significantly impact semiconductor yield.

AI algorithms analyze fabrication data to:

- Detect process anomalies
- Predict defects
- Improve yield rates
- Optimize manufacturing parameters

This results in lower production costs and higher device reliability.

V. Case Study: Reinforcement Learning For Chip Floor Planning

Objective

To evaluate the effectiveness of Reinforcement Learning in optimizing chip floor planning compared with traditional heuristic algorithms.

A. Methodology

The study employs a Reinforcement Learning agent that learns optimal placement strategies through iterative simulations.

1) Input Parameters

- Block dimensions
- Connectivity information
- Timing constraints
- Area requirements

2) Performance Metrics

- Total chip area
- Wire length
- Routing congestion
- Timing performance

B. Results

Table 1 compares traditional floor planning methods with AI-assisted floor planning.

Table 1. Comparative Analysis

Parameter	Traditional Method	AI-based method
Design Time	High	Low
Wire length	Moderate	Reduced

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Table 2

Parameter	Traditional method	AI-based method
Congestion	Higher	Lower
Timing Performance	Good	Improved
Scalability	Limited	High

The AI-based approach demonstrated significant improvements in placement quality and overall design efficiency.

VI. Industrial Applications

AI-assisted VLSI design is increasingly adopted in semiconductor industries for:

1) Automated Physical Design

Machine learning accelerates placement, routing, and timing optimization.

2) AI Hardware Accelerators

Dedicated VLSI architectures are designed to support deep learning workloads.

3) Predictive Design Analytics

AI predicts design bottlenecks before fabrication.

4) Smart Verification Platforms

Machine learning reduces verification effort and accelerates product development.

VII. Future Research Directions

Future advancements are expected in the following areas:

A. Generative AI for RTL Design

Automatic generation of synthesizable Verilog and VHDL code from high-level specifications.

B. Autonomous Chip Design

Fully automated chip development systems capable of making design decisions with minimal human intervention.

C. AI-Driven Timing Closure

Machine learning models for rapid timing prediction and optimization.

D. AI-Assisted 3D IC Design

Optimization of advanced packaging and three-dimensional integrated circuits.

E. Hardware Security

Machine learning techniques for Trojan detection and secure hardware design.

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IX. Conclusion

Artificial Intelligence is transforming Digital VLSI design by introducing intelligent automation into every stage of the design flow. AI-assisted methodologies improve floor planning, routing, power optimization, verification, and manufacturing efficiency. The case study demonstrates that Reinforcement Learning-based floor planning achieves superior performance compared to traditional approaches. As semiconductor complexity continues to grow, AI-driven Electronic Design Automation tools will become essential for designing next-generation integrated circuits.

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