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Unrolled and Pipelined Architectures for Efficient Encoding Decoding of Polar Codes: A Review

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***Abstract*— Polar codes have emerged as a powerful forward error correction technique due to their capacity-achieving performance and adoption in modern communication standards such as 5G. However, the practical implementation of polar code encoders and decoders faces challenges related to latency, throughput, and hardware complexity. This review presents a comprehensive analysis of unrolled and pipelined architectures for efficient encoding and decoding of polar codes, focusing on their design principles, performance trade-offs, and hardware implementation aspects. Unrolled architectures enable ultra-low latency by fully unfolding the decoding process, while pipelined architectures improve throughput through parallel processing stages with balanced resource utilization. The review highlights recent advancements, compares architectural efficiencies in terms of speed, area, and power consumption, and discusses their suitability for high-speed and low-latency communication systems, providing valuable insights for next-generation wireless and error-control coding applications.**

Keywords*— Polar Codes, Unrolled Architecture, Pipelined Architecture, Encoder Design, Decoder Design, High-Throughput Communication Systems.

I. INTRODUCTION

The rapid growth of high-speed wireless communication systems, data-intensive applications, and emerging technologies such as 5G, beyond-5G (B5G), and future 6G networks has placed stringent requirements on error control coding schemes. These systems demand high throughput, ultra-low latency, and energy-efficient hardware implementations to support reliable data transmission over noisy channels[1]. Among various forward error correction (FEC) techniques, polar codes have gained significant attention due to their theoretical ability to achieve channel capacity and their successful adoption in modern communication standards. However, despite their strong error-correcting performance, the practical realization of polar code encoders and decoders remains a challenging task, particularly when stringent latency and throughput constraints must be met[2].

Traditional polar code encoding and decoding architectures, such as successive cancellation (SC) and successive cancellation list (SCL) decoding, often suffer from inherent sequential processing[3]. This sequential nature leads to increased decoding latency and limits achievable throughput, making conventional implementations less suitable for real-time and high-data-rate applications. As communication systems evolve toward supporting ultra-reliable low-latency communication (URLLC) and enhanced mobile broadband (eMBB), there is a critical need for architectural innovations that can overcome these limitations while maintaining reasonable hardware complexity and power consumption[4].

To address these challenges, unrolled and pipelined architectures have emerged as promising design approaches for efficient polar code encoding and decoding. Unrolled architectures aim to completely unfold the decoding or encoding process in hardware, mapping each operation directly to dedicated processing elements. This approach eliminates iterative control overhead and enables extremely low-latency operation, often achieving one-frame-per-cycle processing[5]. As a result, unrolled designs are particularly attractive for applications requiring deterministic and ultra-fast response times. However, such architectures typically come at the cost of increased area and resource utilization, necessitating careful design trade-offs[6].

Pipelined architectures focus on improving throughput by dividing the encoding or decoding process into multiple stages, where different frames or code blocks are processed simultaneously at different pipeline levels. By exploiting parallelism and balanced stage design, pipelined implementations significantly enhance throughput while offering better scalability and resource efficiency compared to fully unrolled designs[7]. Pipelining also provides flexibility in optimizing performance metrics such as clock frequency, latency, and power consumption, making it suitable for a wide range of hardware platforms, including FPGAs and ASICs[8].

In recent years, extensive research has been conducted to optimize unrolled and pipelined architectures for polar codes, exploring aspects such as memory organization, processing element design, scheduling strategies, and quantization techniques[9]. These studies highlight important trade-offs between latency, throughput, silicon area, and energy efficiency. Furthermore, hybrid approaches that combine partial unrolling with pipelining have been proposed to achieve balanced performance suitable for practical deployment in next-generation communication systems[10].

This review focuses on the design principles, operational characteristics, and performance evaluation of unrolled and pipelined architectures for efficient encoding and decoding of polar codes. By systematically analyzing existing architectural approaches and their advantages and limitations, the review aims to provide a clear understanding of how these architectures contribute to meeting the demanding requirements of modern and future communication systems[11]. Such insights are valuable for researchers and engineers involved in the development of high-speed, low-latency, and energy-efficient error control coding hardware[12].

II. LITERATURE REVIEW

Y. Pola et al. [1] presented the design and hardware implementation of polar codes using Verilog for digital communication systems. The work focused on developing a synthesizable polar encoder and decoder suitable for FPGA implementation. The presented architecture emphasized modularity and scalability for different code lengths. Functional verification and synthesis results validated correct operation. The implementation achieved reliable encoding and decoding with reduced hardware complexity. Timing analysis showed stable performance at moderate clock frequencies. The study demonstrated the feasibility of practical polar code hardware realization.

Hebbar et al. [2] presented *DeepPolar*, a novel approach for inventing nonlinear large-kernel polar codes using deep learning techniques. The study leveraged neural networks to optimize kernel structures beyond conventional linear designs. The presented method improved error-correction performance compared to classical polar codes. Simulation results showed noticeable BER gains under identical channel conditions. Although not hardware-focused, the work highlighted future architectural challenges. The study opened new directions for learning-assisted polar code design. It emphasized the need for adaptable encoder–decoder architectures.

Nakul et al. [3] presented a row-wise Hamming code architecture aimed at memory protection applications. The work focused on error detection and correction with low redundancy overhead. The presented architecture achieved fast encoding and decoding suitable for memory subsystems. Hardware analysis showed reduced latency compared to conventional Hamming implementations. Although not specific to polar codes, the design principles are relevant to pipelined ECC architectures. The study demonstrated efficient fault tolerance. It provided useful insights for memory-integrated coding schemes.

Chiu [4] presented an in-depth analysis and design of polar-coded modulation schemes. The study combined modulation and coding to improve spectral efficiency. Analytical and simulation-based evaluations were carried out under different channel conditions. The presented results showed improved throughput and reliability compared to separate coding–modulation approaches. The work highlighted decoding complexity challenges at higher modulation orders. Architectural implications for decoder design were discussed. This study provided a strong theoretical foundation for advanced polar code implementations.

Kam et al. [5] presented an ultra-low-latency successive cancellation polar decoding architecture using tree-level parallelism. The architecture exploited inherent decoding tree structures to enable parallel computation. The presented design significantly reduced decoding latency compared to conventional SC decoders. Hardware synthesis showed improved throughput with manageable area overhead. The decoder achieved latency reductions of more than 40% in comparison benchmarks. Power efficiency was also improved due to reduced clock cycles. This work strongly supports unrolled decoding concepts.

Ji et al. [6] presented an automatic generation framework for pipelined belief propagation polar decoders. The framework enabled flexible decoder construction for varying code lengths and rates. Pipelining was used to enhance throughput while maintaining decoding accuracy. The presented architectures achieved multi-Gbps throughput in ASIC implementations. Hardware evaluation showed balanced trade-offs between area and speed. The work emphasized design automation for scalable decoders. It validated the effectiveness of pipelined polar decoding architectures.

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Song et al. [7] presented a general construction method and efficient encoder implementation for polar codes. The study addressed encoder scalability and parallelism. The presented encoder architecture reduced critical path delay through structured processing. Hardware synthesis results showed high-speed operation with reduced logic depth. The design supported flexible code rates and lengths. The work demonstrated improved encoder efficiency over conventional recursive designs. It contributed to high-throughput polar encoder development.

Kavipriya and Maheswari [8] presented a high-speed polar encoder architecture using a radix-k processing engine for 5G applications. The radix-k approach enabled parallel computation of encoding stages. The presented encoder achieved significantly higher throughput than radix-2 designs. Hardware results indicated reduced latency and improved clock frequency. The design was optimized for next-generation wireless standards. Area utilization remained within acceptable limits. The study validated the suitability of parallel encoder architectures for 5G.

Shrestha et al. [9] presented a high-throughput and high-speed polar decoder VLSI architecture for 5G New Radio. The architecture employed aggressive pipelining and parallel processing. The presented decoder achieved throughput in the order of several Gbps. Latency was significantly reduced compared to baseline architectures. Hardware synthesis demonstrated efficient resource utilization. The design supported practical 5G code configurations. This work highlighted the importance of pipelined decoding for real-time systems.

Yoon and Kim [10] presented a generalized tree architecture for efficient successive cancellation polar decoding. The architecture restructured decoding operations to reduce control overhead. The presented approach improved hardware utilization and decoding speed. Synthesis results showed reduced area and power consumption. Latency improvements were achieved through structured computation reuse. The design supported flexible code lengths. This work provided a foundation for optimized SC decoder implementations.

Liang et al. [11] presented a joint list polar decoder combining successive cancellation and sphere decoding. The hybrid approach aimed to improve decoding performance at moderate list sizes. The presented decoder achieved lower error rates compared to conventional SCL decoders. Complexity analysis showed manageable overhead for improved performance. The work highlighted architectural challenges in combining decoding strategies. Hardware feasibility was discussed for high-speed systems. The study contributed to performance-oriented decoder designs.

Mousavi et al. [12] presented efficient partial-sum network architectures for list successive cancellation decoding of polar codes. The design addressed one of the major bottlenecks in SCL decoders. The presented architecture reduced memory access and routing complexity. Hardware evaluations showed improved throughput and lower power consumption. Latency was reduced without degrading decoding performance. The work enabled scalable list decoding implementations. It remains highly relevant for unrolled and pipelined polar decoder designs.

Table 1: Summary of literature review

Sr. No.	Author	Year	Work	Outcome
1	Pola	2025	Design and Hardware Implementation of Polar Codes Using Verilog for Digital Systems	Demonstrated feasible FPGA-based polar encoder–decoder with stable performance and reduced hardware complexity.
2	Hebbar	2024	DeepPolar: Inventing Nonlinear Large-Kernel Polar Codes via Deep Learning	Achieved improved BER performance by learning optimized nonlinear polar code kernels using deep learning.
3	Nakul	2024	Row-wise Hamming Code for Memory Applications	Provided low-latency and area-efficient error correction suitable for memory protection

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				systems.
4	Chiu	2022	Analysis and Design of Polar-Coded Modulation	Improved spectral efficiency and reliability through joint modulation and polar coding techniques.
5	Kam	2021	Ultralow-Latency SC Polar Decoding Using Tree-Level Parallelism	Achieved significant latency reduction using parallel tree-level decoding architecture.
6	Ji	2020	Autogeneration of Pipelined Belief Propagation Polar Decoders	Enabled high-throughput pipelined polar decoders with automated architecture generation.
7	Song	2020	General Construction and Encoder Implementation of Polar Codes	Developed a scalable and high-speed polar encoder with reduced critical path delay.
8	Kavi priya	2019	High-Speed Polar Encoder Using Radix-k Processing Engine	Achieved high throughput and low latency suitable for 5G communication systems.
9	Shre stha	2019	High-Throughput Polar Decoder VLSI Architecture for 5G NR	Demonstrated multi-Gbps decoding throughput with efficient pipelined VLSI design.
10	Yoo n	2018	Generalized Tree Architecture for SC Polar Decoding	Improved decoding efficiency with reduced area and power consumption.
11	Lian g	2018	Joint List Polar Decoder with SC and Sphere Decoding	Enhanced decoding performance with lower error rates using hybrid decoding strategies.
12	Mou savi	2018	Efficient Partial-Sum Network Architectures for SCL Decoding	Reduced memory and routing overhead in list-based polar decoders while improving throughput.

III. CHALLENGES

Although unrolled and pipelined architectures significantly improve the throughput and latency performance of polar code encoding and decoding, several challenges remain that restrict their efficient and scalable implementation in practical systems. These challenges arise mainly from hardware constraints, design complexity, and the need to balance performance with flexibility and power efficiency. Addressing these issues is essential for deploying polar code architectures in real-time, high-speed communication systems such as 5G, B5G, and future 6G networks.

1. **High hardware resource utilization:** Fully unrolled architectures require a large number of processing elements and logic blocks, which leads to high utilization of hardware resources. This significantly increases silicon area, making such designs expensive and less suitable for cost-sensitive applications.

2. **Increased power consumption:** Extensive parallelism and continuous operation of multiple processing units in unrolled and deeply pipelined architectures result in higher dynamic and static power consumption. This poses challenges for battery-powered and energy-constrained devices.
3. **Limited scalability for variable code parameters:** Many unrolled designs are optimized for fixed code lengths and rates. Modifying these parameters often requires redesigning the hardware, which limits scalability and flexibility in adaptive communication systems.
4. **Routing and interconnect complexity:** As the level of parallelism increases, routing congestion and long interconnect paths become critical issues. These factors can degrade timing performance and limit achievable clock frequencies in pipelined architectures.
5. **Memory access bottlenecks:** Frequent access to log-likelihood ratios (LLRs) and partial-sum memories can create bottlenecks, especially in high-throughput decoders. Inefficient memory organization can increase latency and power consumption.
6. **Latency versus accuracy trade-offs:** Aggressive parallel and pipelined decoding techniques may simplify computations to reduce latency, which can negatively impact decoding accuracy. Maintaining error-correction performance while minimizing delay remains a key challenge.
7. **Complexity of advanced decoding schemes:** Supporting advanced decoding algorithms such as successive cancellation list (SCL) and belief propagation increases architectural complexity. These schemes require additional memory, control logic, and processing resources.
8. **Portability across hardware platforms:** Designs optimized for ASIC implementations may not map efficiently onto FPGA platforms, and vice versa. Achieving performance portability while maintaining high throughput and low latency across different hardware technologies is challenging.

IV. CONCLUSION

Unrolled and pipelined architectures have emerged as highly effective solutions for addressing the stringent throughput and latency requirements of polar code encoding and decoding in modern communication systems. By exploiting parallelism and structured processing, these architectures significantly enhance performance compared to conventional implementations, making them suitable for applications such as 5G and beyond. However, their practical realization involves critical trade-offs among hardware complexity, power consumption, scalability, and design flexibility. While unrolled architectures offer ultra-low latency and deterministic performance, pipelined designs provide better resource efficiency and adaptability. Therefore, a balanced architectural approach—potentially combining partial unrolling with optimized pipelining—represents a promising direction for achieving high-speed, energy-efficient, and scalable polar code hardware implementations for next-generation wireless communication systems.

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