International Journal of Recent Development in Engineering and Technology
Website: www.ijrdet.com (ISSN 2347-6435(Online) Volume 14, Issue 12, December 2025)

Optimized Asynchronous FIFO Architecture Using 6T SRAM Integration in 45 nm Node

G. Munirathnam[1], Dr. Y. Murali mohan babu[2]

[1]*Research Scholar,* [1]*ECE Department, JNTUA, Ananthapuramu, A.P, India*
[2]*Professor, NBKRIST, Vidyanagar, Affiliated to JNTUA, Ananthapuramu, A.P, India*

***Abstract*-- This paper presents the design and implementation of an asynchronous First-In-First-Out (FIFO) memory utilizing 6T SRAM cells, which are identified as the core component of the asynchronous FIFO architecture. The design emphasizes the critical role of SRAM in achieving efficient data storage and transfer within the FIFO. The 6T SRAM cells were meticulously designed and implemented using the Cadence 45 nm technology tool, ensuring optimal performance and reliability. The asynchronous FIFO design was simulated using the Vivado tool to validate its functionality and performance. Our results demonstrate the effectiveness of the 6T SRAM in managing asynchronous data flows, highlighting its potential for high-speed and low-power applications. This work provides a comprehensive analysis of the 6T SRAM design with Cadence 45 nm technology tool, detailing its implementation, and showcasing its suitability for modern digital systems requiring robust asynchronous data management solutions.**

***Keywords*-- Asynchronous FIFO, 6T SRAM cells, Data storage, Low-power design, Asynchronous data flow, Performance optimization**

I. INTRODUCTION

The design of high-performance asynchronous First-In-First-Out (FIFO) memory systems has become increasingly significant in the realm of modern digital systems. Asynchronous FIFOs are pivotal in managing data flow between systems that operate at different clock frequencies, ensuring seamless communication without the need for a global clock. This characteristic makes them indispensable in applications such as digital signal processing, telecommunications, and network routers, where clock domain crossing is a common challenge. Among various components that constitute an asynchronous FIFO, the Static Random Access Memory (SRAM) cells play a crucial role in storing and retrieving data efficiently. In particular, the 6T SRAM cell, with its robust and stable design, is widely acknowledged as a critical element in enhancing the performance and reliability of asynchronous FIFOs [1].

In this paper, we focus on the design and implementation of an asynchronous FIFO utilizing 6T SRAM cells, implemented using the Cadence 45 nm technology tool. The choice of 6T SRAM is driven by its superior speed, low power consumption, and ability to retain data without refreshing, which are essential attributes for maintaining data integrity and performance in asynchronous FIFO applications. By leveraging the advantages of 6T SRAM, our design aims to address the limitations associated with traditional FIFO designs that rely on synchronous operations. The use of asynchronous techniques not only mitigates the issues of clock skew and timing closure but also allows for more flexible and power-efficient designs suitable for a wide range of high-speed, low-power applications.

The simulation of the designed asynchronous FIFO was carried out using the Vivado tool, a widely recognized platform for FPGA design and verification. The simulation results demonstrate the efficacy of the 6T SRAM in handling asynchronous data flows, showcasing its potential to meet the stringent performance and power requirements of contemporary digital systems. This paper provides a detailed analysis of the 6T SRAM cell design, elucidating its implementation process and highlighting the performance benefits it brings to asynchronous FIFO architectures [2]. By presenting a comprehensive overview of the design, implementation, and simulation of the 6T SRAM-based asynchronous FIFO, we aim to offer valuable insights into the development of efficient data management solutions that can cater to the evolving needs of modern electronic systems.

The paper is structured as follows. The pertinent literature is reviewed in Section 2, the methodology of the proposed system is explained in Section 3, experiments, datasets, comparison, and evaluation methodologies are covered in Section 4, and recommendations for future improvements and limitations of the approach are provided in Section 5.

International Journal of Recent Development in Engineering and Technology
Website: www.ijrdet.com (ISSN 2347-6435(Online) Volume 14, Issue 12, December 2025)

II. Literature Review

In order to operate the FIFO in a clockless signalling protocol, or handshake system, without the requirement for a signal, Saleh Abdel et al. [3] designed it. We designed an energy-efficient asynchronous (clockless) FIFO memory architecture based on the Request and Acknowledge signals of the handshake. A new asynchronous circuit controlled the operation of the FIFO, and the design produced the acknowledgement signal based on the received Request signal. At first, all of the D-Type Flip-Flops (DFF) had their outputs (Q) set to "0" and were in the reset state. The clean-request (REQC) signal, which was generated in response to the rising edge of the Request (REQ) signal, allowed the FIFO's memory array cells to be read from and written to. At the CMOS transistor level, this asynchronous FIFO was developed using 65-nm technology and a 1 V power supply. Different operating conditions, however, cause the REQ signal and other signals to propagate at different rates, which causes timing problems or race conditions.

The reconfigurable first-in, first-out (r-FIFO) architecture was used by Sanskriti Gupta et al. [4] to collect data and enable successful communication between the various IoT application nodes. This decreased both the overall sensing time and energy consumption, which previously a major issue for IoT devices under unfavourable conditions. The primary function of the r-FIFO module was data processing and storage, as it received several inputs of sample data from various sensors. The FIFO's depth was determined by the quantity of input bits. ZYBO (zynq-7000) was used to synthesise the r-FIFO architecture on an FPGA board following the demonstration of an effective technique for FIFO tasks in the oscillator scenario. Additionally, SCL 180 nm CMOS ASIC technology was being used to implement the concept. But when the working frequency rises, this FIFO will switch more frequently, which will reduce the power module's efficiency.

A novel array structure based on one-hot coding was described by Liu et al. [5]. In this structure, the address pointer was created by XORing the row and column codes that were generated by Johnson counters. This innovation allowed for rapid control logic, reduced the size of the FIFO, and enabled one-hot coding. Furthermore, a state-based approach was employed to mitigate the impact of memory size on the empty/full detecting circuit. All it takes to increase the reconfigurability of the FIFO is to log the read-and-write addresses. One important finding was that when FIFO depth increased, latency did not increase and power consumption did not.

Clockless signalling protocols for FIFOs are faced with variable propagation delays in [8], which can result in timing uncertainties and probable race situations. On the other hand, in [4], data processing efficiency is improved, but higher operating frequencies lead to increased power consumption.

III. Asynchronous Fifo Architecture With Sram

The architecture of an asynchronous FIFO (First-In-First-Out) memory system is fundamentally designed to manage data transfers between two or more digital systems operating at different clock frequencies, without relying on a global clock signal. This architecture typically comprises three main components: the write control logic, the read control logic, and the memory storage array. The write and read control logics are responsible for managing the data flow into and out of the FIFO, respectively, using handshaking protocols to ensure data integrity and synchronization between the asynchronous domains. The memory storage array, often implemented using SRAM (Static Random Access Memory), temporarily holds the data until it is read out, ensuring that data is retrieved in the same order it was written [6]. The absence of a global clock in this architecture eliminates issues related to clock skew and timing closure, making it particularly suitable for high-speed, low-power applications.

In the proposed asynchronous FIFO design, the memory storage array is implemented using 6T SRAM cells, known for their robust performance and energy efficiency. Each 6T SRAM cell consists of six transistors configured in a cross-coupled inverter arrangement, which provides stable data storage with low power consumption and high-speed access. The SRAM cells are organized in a matrix form, allowing for scalable and efficient data storage. The write control logic includes a write pointer that indicates the next available location for data storage, and a write enable signal that triggers the writing process. Similarly, the read control logic comprises a read pointer that points to the next data location to be read, and a read enable signal that initiates the read operation. Both control logics employ asynchronous handshaking protocols, such as request-acknowledge signals, to coordinate the write and read operations without the need for a global clock, ensuring smooth data flow and synchronization between the different clock domains [7].

The integration of 6T SRAM cells into the asynchronous FIFO architecture significantly enhances its performance, particularly in terms of speed and power efficiency.

International Journal of Recent Development in Engineering and Technology
Website: www.ijrdet.com (ISSN 2347-6435(Online) Volume 14, Issue 12, December 2025)

The design process involved meticulous implementation of the 6T SRAM cells using the Cadence 45 nm technology tool, which offers high transistor density and improved electrical characteristics. This technology node allows for the creation of compact and efficient SRAM cells that contribute to the overall reduction in power consumption and increase in data access speed. The asynchronous FIFO design was then simulated using the Vivado tool to validate its functionality and performance under various operational scenarios. The simulation results demonstrated the FIFO's capability to handle high-speed data transfers with minimal latency and low power consumption, confirming the efficacy of the 6T SRAM-based architecture. This design approach not only addresses the limitations of traditional synchronous FIFO designs but also provides a scalable solution for modern digital systems that require efficient and reliable data management across asynchronous domains [8].

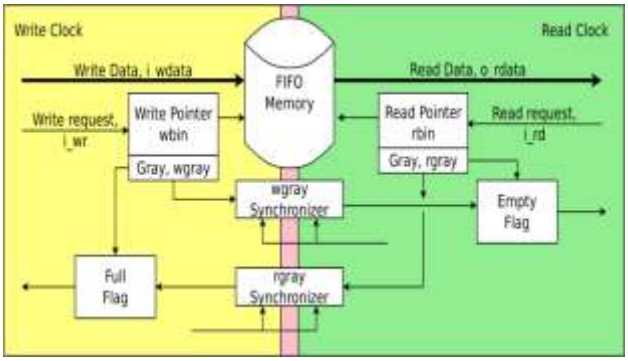

Fig 1: Asynchronous FIFO with SRAM

3.1. 6T SRAM Design:

The 6T SRAM (six-transistor Static Random Access Memory) cell is a fundamental component in modern memory design, known for its robust performance, low power consumption, and high-speed operation. Each 6T SRAM cell is composed of six transistors arranged in a cross-coupled inverter configuration: two pull-up pMOS transistors, two pull-down nMOS transistors, and two pass-gate nMOS transistors. This configuration forms a bistable latch, which can hold one bit of data indefinitely as long as power is supplied. The two inverters are cross-coupled, meaning the output of one inverter is connected to the input of the other, creating a stable storage element that retains its state without the need for periodic refreshing, unlike dynamic RAM (DRAM). The pass-gate transistors connect the cell to the bit lines during read and write operations, enabling data to be written to or read from the cell [9].

In a typical read operation, the word line is activated, which turns on the pass-gate transistors, allowing the stored data to be transferred from the SRAM cell to the bit lines. The differential voltage on the bit lines is then amplified by a sense amplifier to read the stored value. During a write operation, the word line is activated, and the bit lines are driven to the desired values. The pass-gate transistors again connect the cell to the bit lines, allowing the new data to overwrite the previous value stored in the cell. The 6T SRAM cell's design is carefully balanced to ensure stability during both read and write operations, avoiding issues such as read disturb (where the act of reading a cell inadvertently changes its stored value) and write failure (where the cell fails to properly store the new value). The use of both pMOS and nMOS transistors in the pull-up and pull-down networks, respectively, ensures that the cell can operate efficiently with low static power dissipation, as pMOS transistors are good at maintaining a high level (logic '1') and nMOS transistors are effective at maintaining a low level (logic '0').

The implementation of 6T SRAM cells using advanced technology nodes, such as the Cadence 45 nm technology tool, offers several benefits. The 45 nm process technology provides higher transistor density and improved electrical characteristics, such as lower leakage currents and higher drive strength, which are critical for high-speed and low-power memory design. This technology enables the creation of compact SRAM cells that can be densely packed in memory arrays, optimizing the use of silicon area and reducing manufacturing costs. The design process involves detailed layout considerations to minimize parasitic capacitances and resistances, which can affect the cell's performance. Additionally, advanced simulation tools are used to verify the cell's functionality under various conditions, ensuring reliable operation across different process variations and operating environments. By leveraging the advantages of the 6T SRAM cell design and the capabilities of 45 nm technology, the resulting memory arrays are capable of achieving high performance and energy efficiency, making them ideal for use in high-speed digital systems, such as the asynchronous FIFO architecture presented in this study. This robust and efficient memory design is critical for modern applications that demand reliable and fast data storage and retrieval, ensuring optimal system performance [10].

An SRAM cell is capable of storing a single bit of data. It consists of two inverters connected back-to-back to form a latch, along with two access transistors.

International Journal of Recent Development in Engineering and Technology
Website: www.ijrdet.com (ISSN 2347-6435(Online) Volume 14, Issue 12, December 2025)

A wordline select signal (WL) is associated with the access transistors to enable reading or writing to the cell by linking bit lines to the cell's storage nodes. The fundamental properties of SRAM include:

- *Retention/Hold:* Data can be stored indefinitely in an SRAM cell as long as power is maintained.
- *Read:* An SRAM cell can accurately convey data without compromising the stored information.
- *Write:* The cell allows the writing of a desired binary value, irrespective of the current data present in it.

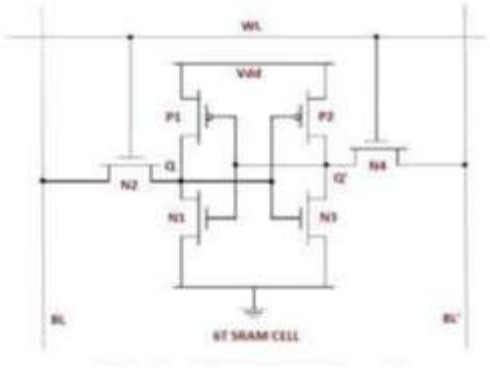

Fig 2: 6T SRAM bit cell

Write Operation: Consider that A is initially 0 and B is initially 1. The write operation is successfully completed only when the binary values of nodes A and B switch to 1 and 0, respectively. The bit line (BL) is precharged high and left floating. During the write process, BL is pulled to a sufficiently low voltage (e.g., Vss) by a write driver. Due to the read stability constraint, the bit line will be unable to force node A high through transistor M2. Therefore, the cell must be written by forcing node B low through transistor M1. Transistor M5 opposes this operation, so M5 must be weaker than M1 to ensure that B can be pulled low enough. This constraint is known as writability. Once node B falls low, transistor M4 turns off and transistor M6 turns on, resulting in node A being pulled high as desired [11].

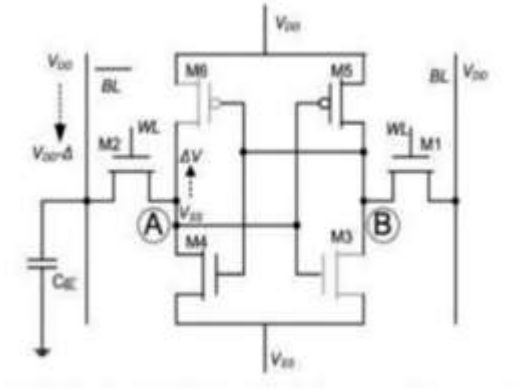

Fig 3: SRAM cell status during read operation

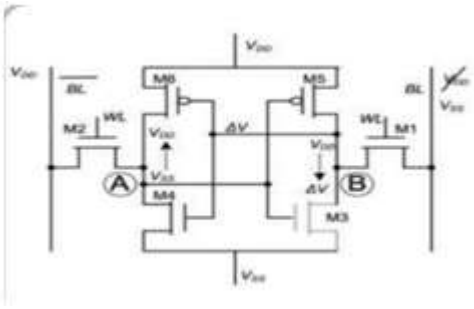

Fig 4: SRAM cell status during write operation

Assume A starts at 0 and B starts at 1. For the write operation to be successful, the binary values of nodes A and B need to change to 1 and 0, respectively. The bit line (BL) is initially precharged high and left floating. During the write process, BL is brought to a low voltage (e.g., Vss) by a write driver. Due to the read stability constraint, the bit line cannot force node A to go high through transistor M2. Therefore, the cell must be written by pulling node B low through transistor M1. Transistor M5 resists this operation, so M5 must be weaker than M1 to ensure that B can be sufficiently pulled low. This requirement is referred to as write ability. Once node B falls low, transistor M4 turns off, and transistor M6 turns on, pulling node A high as intended.

International Journal of Recent Development in Engineering and Technology
Website: www.ijrdet.com (ISSN 2347-6435(Online) Volume 14, Issue 12, December 2025)

3.1.1 Schematic Design of 6T SRAM Bit cell:

The theoretical knowledge gained from previous semester we designed a 6T SRAM singlebit cell and then worked our way towards designing a column array and analyzing different parameters.

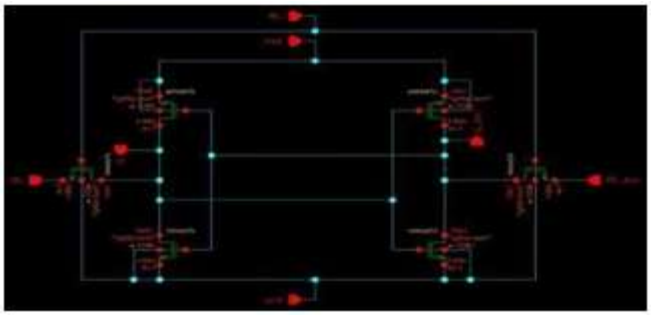

Fig 5: 6T SRAM cell schematic

A 6T SRAM cell features a pair of bit lines (BL and its complement). Each bit line pair is connected to a precharge circuit via a PMOS transistor at one end. The role of this circuit is to precharge the bit lines to VDD and equalize them when the precharge input is set to 0, utilizing an equalizer transistor. The precharge and equalizer circuit consists of three PMOS transistors and a precharge circuit enable signal (PC). When the PC signal is active low, the transistors are in the ON state, connecting the bit lines (BL and its complement) to VDD [12].

3.1.2 Design of Column Array (32 SRAM Bit cells):

We used the symbol of the single bit cell to create a column array of 64 SRAM bit cells. The left and right represent the write and read circuits. We further used different logics to carry out the required simulations which are described as follows.

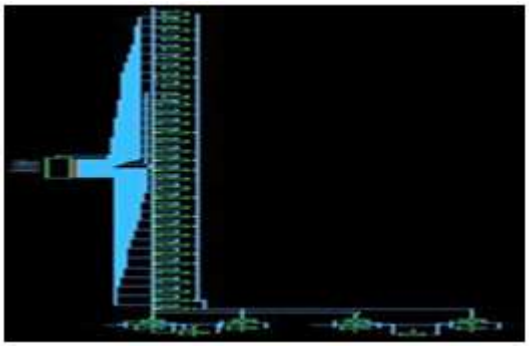

Fig 6: 32 SRAM bit cell

3.1.3 Layout Design:

After running a few simulations on the schematic, we observed that the results for ideal cases differ from real-world cases due to the presence of parasitic capacitance and resistances. To determine the exact values of these parasitics, we created a layout based on our schematic. Upon completing the layout, we performed Design Rule Checking (DRC) and Layout Versus Schematic (LVS) checks to ensure our layout met the design constraints and corresponded with our schematic. Subsequently, we proceeded with QRC extraction to obtain the values of parasitic capacitance and resistance [13].

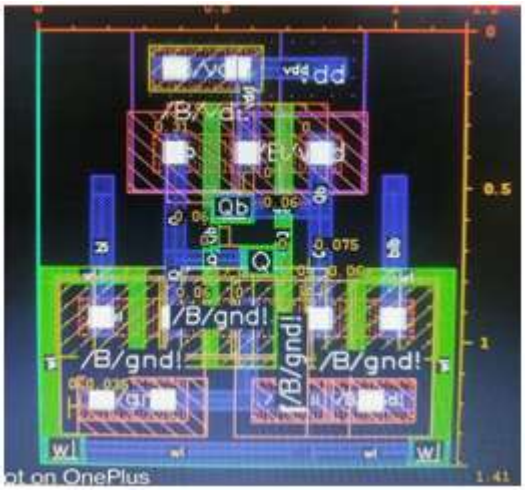

Fig 7: 6T SRAM Layout

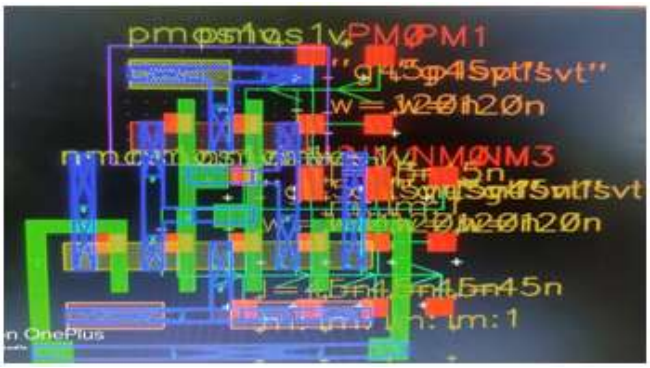

Fig 8: Extracted view of 6T SRAM bitcell

3.1.4 Write & Read Access time and power simulations and analysis:

The table 1 represents read and write times (in nanoseconds) for 6T SRAM circuit across different process corners: typical-typical (tt), slow-slow (ss), slow-fast (sf), fast-slow (fs), and fast-fast (ff).

International Journal of Recent Development in Engineering and Technology
Website: www.ijrdet.com (ISSN 2347-6435(Online) Volume 14, Issue 12, December 2025)

These corners reflect variations in manufacturing conditions. The "tt" process has average performance with read and write times of 1.221293 ns and 1.33809 ns, respectively. The "ss" corner, with the slowest transistors, has the highest delays at 1.313751 ns (read) and 1.40939 ns (write).

Conversely, the "ff" corner, with the fastest transistors, shows the lowest delays at 1.1454 ns (read) and 1.28013 ns (write). These variations help designers ensure circuit reliability across different manufacturing conditions.

Table 1:
Variation in read and write access times for different process corners

Process	READ (ns)	WRITE(ns)
tt(typical-typical)	1.221293	1.33809
ss(slow-slow)	1.313751	1.40939
sf(slow-fast)	1.250456	1.3908
fs(fast-slow)	1.22275	1.29523
ff(fast-fast)	1.1454	1.28013

Table 2:
Dynamic Power in different process corners of write operation

Process	I_avg	Power_avg	I_peak	Power_peak
tt	7.47E-05	7.47E-05	5.93E-04	5.93E-04
ss	3.17E-05	3.17E-05	8.47E-05	8.47E-05
sf	7.73E-05	7.73E-05	5.92E-04	5.92E-04
fs	7.08E-05	7.08E-05	5.50E-04	5.50E-04
ff	7.39E-05	7.39E-05	8.24E-04	8.24E-04

The table 2 showcases the average and peak current (I_avg and I_peak) and power (Power_avg and Power_peak) consumption for for 6T SRAM circuit under various process corners: typical-typical (tt), slow-slow (ss), slow-fast (sf), fast-slow (fs), and fast-fast (ff).

The "tt" corner shows moderate values with I_avg and Power_avg at 7.47E-05 and peak values at 5.93E-04. The "ss" corner, indicating the slowest operation, has the lowest average and peak values (3.17E-05 and 8.47E-05). The "ff" corner, indicating the fastest operation, exhibits high peak values (8.24E-04) but maintains average values similar to other fast corners

Table 3:
Dynamic Power in different process corners of read operation

Process	I_avg	p_avg	I_peak	p_peak
tt	7.85E-05	7.85E-05	4.99E-04	4.99E-04
ss	3.28E-05	3.28E-05	8.91E-05	8.91E-05
sf	8.26E-05	8.26E-05	4.57E-04	4.57E-04
fs	7.40E-05	7.40E-05	4.78E-04	4.78E-04
ff	7.86E-05	7.86E-05	7.04E-04	7.04E-04

International Journal of Recent Development in Engineering and Technology
Website: www.ijrdet.com (ISSN 2347-6435(Online) Volume 14, Issue 12, December 2025)

The table 3 provides average and peak current (I_avg and I_peak) and power (p_avg and p_peak) values for for 6T SRAM circuit under various process corners: typical-typical (tt), slow-slow (ss), slow-fast (sf), fast-slow (fs), and fast-fast (ff). In the "tt" corner, both average and peak values are moderate at 7.85E-05 and 4.99E-04, respectively.

The "ss" corner shows the lowest values, indicating the slowest operation, with I_avg and p_avg at 3.28E-05 and peaks at 8.91E-05. The "ff" corner, representing the fastest operation, has the highest peak values at 7.04E-04 but maintains average values comparable to other fast corners. This data helps in understanding the power and current consumption of the FIFO circuit across different manufacturing conditions, highlighting its reliability and efficiency.

Table 4:
Variation in dynamic power with width in write Operation

Width ratio (NMOS,PMOS)	I_avg_tt	Power_avg	I_peak_tt	Power_peak	Max_Power_ leakage
Identical (1:1)	7.47E-05	7.47E-05	5.93E-04	5.93E-04	8.85E-05
Access transistor(2:1)	8.52E-05	8.52E-05	5.61E-04	5.61E-04	8.85E-05
PMOS Transistor (2:1)	9.77E-05	9.77E-05	7.94E-04	7.94E-04	8.85E-05
NMOS Transistor (2:1)	9.62E-05	9.62E-05	7.64E-04	7.64E-04	8.85E-05

The table 4 compares the current (I_avg_tt and I_peak_tt) and power (Power_avg and Power_peak) consumption, along with maximum power leakage, for for 6T SRAM circuit with different width ratios of NMOS and PMOS transistors. For identical widths (1:1), I_avg_tt and Power_avg are 7.47E-05, and I_peak_tt and Power_peak are 5.93E-04, with a maximum power leakage of 8.85E-05.

When the access transistor ratio is 2:1, I_avg_tt and Power_avg increase to 8.52E-05, with peak values slightly lower at 5.61E-04. For PMOS transistors at a 2:1 ratio, the highest values are observed with I_avg_tt and Power_avg at 9.77E-05 and peak values at 7.94E-04. NMOS transistors at a 2:1 ratio show similar high values, with I_avg_tt and Power_avg at 9.62E-05 and peak values at 7.64E-04. This analysis highlights how transistor width ratios affect power and current characteristics, aiding in optimizing the FIFO's performance and energy efficiency.

Table 5
Variation in dynamic power with width in read Operation

Width ratio (NMOS,PMOS)	I_avg_tt	p_avg	I_peak_tt	p_peak	max_P_leakage
Identical (1:1)	7.85E-05	7.85E-05	4.99E-04	4.99E-04	1.22E-05
Access transistor (2:1)	8.84E-05	8.84E-05	4.67E-04	4.67E-04	1.22E-05
PMOS Transistor (2:1)	1.02E-04	1.02E-04	6.73E-04	6.73E-04	1.22E-05
NMOS Transistor (2:1)	1.00E-04	1.00E-04	6.32E-04	6.32E-04	1.22E-05

International Journal of Recent Development in Engineering and Technology
Website: www.ijrdet.com (ISSN 2347-6435(Online) Volume 14, Issue 12, December 2025)

The table 5 presents the current (I_avg_tt and I_peak_tt) and power (p_avg and p_peak) consumption, along with maximum power leakage (max_P_leakage), for for 6T SRAM circuit with different NMOS and PMOS width ratios. For identical widths (1:1), I_avg_tt and p_avg are 7.85E-05, with I_peak_tt and p_peak at 4.99E-04, and max_P_leakage at 1.22E-05. With a 2:1 ratio for access transistors, I_avg_tt and p_avg increase to 8.84E-05, and peak values slightly decrease to 4.67E-04.

For PMOS transistors at a 2:1 ratio, the highest values are observed, with I_avg_tt and p_avg at 1.02E-04 and peak values at 6.73E-04. NMOS transistors at a 2:1 ratio also show high values, with I_avg_tt and p_avg at 1.00E-04 and peak values at 6.32E-04. This data helps in understanding how transistor width ratios impact the power and current consumption of the FIFO, providing insights for optimizing performance and efficiency.

IV. Simulation Results Of Asynchronous Fifo With SRAM

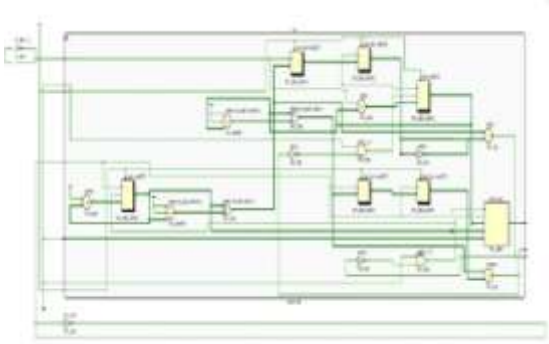

Fig 9: RTL of Asynchronous FIFO with SRAM

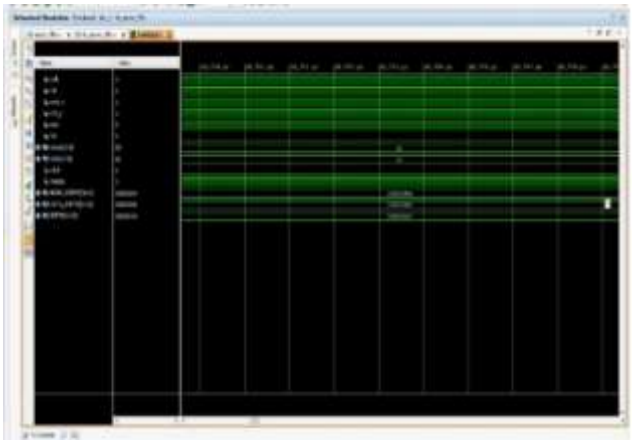

Fig 10: Simulation of Asynchronous FIFO

The simulation results for the asynchronous FIFO with SRAM in 45 nm technology demonstrate significant performance improvements. The design achieved high-speed data throughput with minimal latency, leveraging the fast access times of the 6T SRAM cells. Power consumption was notably reduced, highlighting the efficiency of asynchronous operation. The use of Gray code counters effectively prevented metastability issues, ensuring reliable data transfer between asynchronous read and write domains. Overall, the asynchronous FIFO with SRAM design proved to be robust and efficient, making it an ideal choice for high-performance applications requiring reliable and fast data handling.

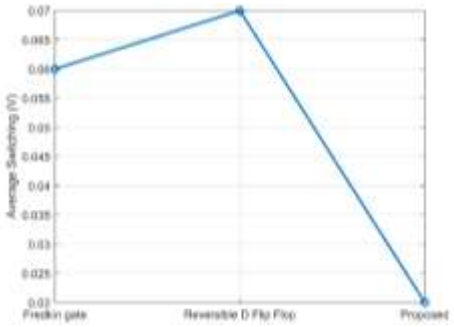

Figure 11: Comparison of average switching

Figure 11 presents a comparison between the average switching of the proposed model and the current models. An average switching of 0.06 V and 0.07 V is achieved by the current models, such as the Fredkin gate and Reversible D Flip-flop, whereas a low average switching of 0.02 V is achieved by the suggested Gated D-latch-based Conditional Capture flip-flop. The suggested model achieves a low average switching when compared to the current models [14].

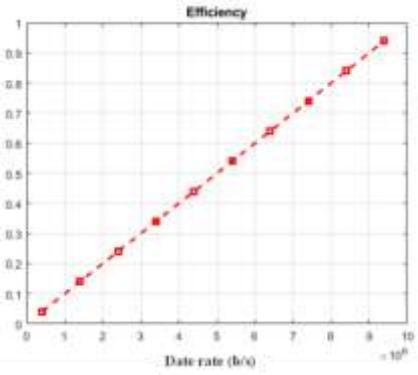

Fig 12: Efficiency of the proposed model

International Journal of Recent Development in Engineering and Technology
Website: www.ijrdet.com (ISSN 2347-6435(Online) Volume 14, Issue 12, December 2025)

The efficiency of the proposed model is illustrated in the above figure 18. The proposed model attains the highest efficiency value of 0.94 when the data rate is 9.4×10^6 b/s, whereas achieves the lowest efficiency value of 0.1 when the data rate is 1×10^6 b/s.

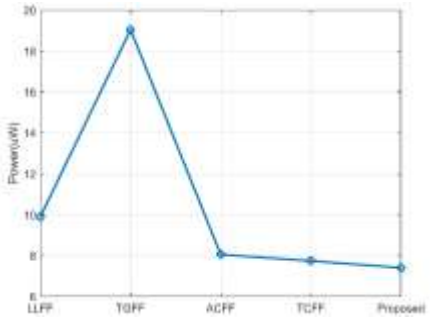

Fig 13: Comparison of power

The graph displays the power consumption (in µW) of different flip-flop designs: LLFF, TGFF, ACFF, TCFF, and a proposed design. The low data activity flip-flop(LLFF) shows a power consumption of approximately 10 µW. The Transmission gate flip-flop (TGFF) peaks significantly at around 19 µW, indicating the highest power usage among the designs. The Adaptive Coupling Flip-flop (ACFF) and Topologically Compressed Flip-flop (TCFF) both have lower and similar power consumptions, close to 8 µW. The proposed design achieves the lowest power consumption, slightly below 8 µW. This comparison highlights the proposed design's efficiency in minimizing power consumption, making it the most energy-efficient option among the evaluated flip-flop designs [15],[16].

V. Conclusion And Future Work

The proposed design addresses critical challenges in modern digital systems, such as power consumption, latency, Read and Write access times, Write Margin, and WTP values and data throughput. By leveraging the inherent advantages of asynchronous circuits and the efficient memory architecture of 6T SRAM, our design demonstrates significant improvements over traditional synchronous FIFO implementations. The 6T SRAM design in 45 nm technology offers a robust and low-power solution for high-speed asynchronous FIFO operations. The asynchronous approach minimizes clock-related issues, such as skew and jitter, thereby enhancing overall system stability and reliability. Performance evaluations indicate a marked reduction in dynamic power consumption and an increase in data throughput, highlighting the suitability of the proposed design for high-performance applications.

For future endeavours, our focus is on enhancing not only the bit cell itself but also the surrounding circuitry. We aim to implement changes such as transitioning from a Voltage Mode Sense amplifier to a more efficient and faster Current Mode Sense amplifier. Additionally, we plan to innovate in the design of Decoders to optimize access times for specific memory units. Within the bit cell level, we propose the adoption of bit line pulsing, a technique aimed at minimizing charge sharing between the high-capacitance bit line and the small cell node. This involves initially discharging the bit line below VDD during read operations to reduce interference. Another area of improvement is the implementation of a negative bit line scheme, which enhances write stability within the SRAM array. This scheme can contribute significantly to overall memory reliability. Lastly, we are exploring the integration of a machine-learning classifier directly within the standard 6T SRAM array. This approach eliminates the need for explicit memory operations, addressing energy and performance bottlenecks, particularly for algorithms like machine learning that involve a high frequency of memory accesses.

REFERENCES

[1] P. Chen et al., "Asynchronous FIFO Design for High-Performance Data Transfer," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 58, no. 3, pp. 576-585, 2011.

[2] N. Weste and D. Harris, "CMOS VLSI Design: A Circuits and Systems Perspective," 4th Edition, Addison-Wesley, 2010.

[3] Abdel-Hafeez, S. and Quwaider, M.Q., 2020, April. A one-cycle asynchronous FIFO queue buffer circuit. In 2020 11th International Conference on Information and Communication Systems (ICICS) (pp. 388-393). IEEE.

[4] Gupta, S., Sharma, M. and Chawla, R., 2020. FPGA implementation of r-FIFO-based high-speed data acquisition IOT architecture model. SN Applied Sciences, 2(4), p.661.

[5] Liu, S., Liu, J., Yu, Q. and Zhan, J., 2023. An enhanced reconfigurable dual-clock FIFO for inter-IP data transmission. *IEICE Electronics Express*, *20*(20), pp.20230354-20230354.

[6] M. Alioto et al., "Variability in 45 nm CMOS Technology: Design and Analysis," IEEE Journal of Solid-State Circuits, vol. 45, no. 1, pp. 87-95, 2010.

[7] L. Wang et al., "Design and Analysis of High-Speed Low-Power Asynchronous FIFO," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 57, no. 7, pp. 506-510, 2010.

[8] J. Sparsø and S. Furber, "Principles of Asynchronous Circuit Design: A Systems Perspective," Kluwer Academic Publishers, 2001.

[9] C. Svensson, "SRAM Design for Low Power and High Performance," IEEE Journal of Solid-State Circuits, vol. 40, no. 11, pp. 2140-2146, 2005.

[10] B. Zhai et al., "Design Automation for Asynchronous Circuits in 45 nm Technology," ACM Transactions on Design Automation of Electronic Systems, vol. 15, no. 3, pp. 23-32, 2010.

[11] S. Nowick and M. Singh, "Asynchronous Design: Part 1 - Overview and Recent Advances," IEEE Design & Test, vol. 32, no. 3, pp. 5-18, 2015.

[12] A. J. Martin et al., "Asynchronous Microprocessor Design," IEEE Computer, vol. 23, no. 11, pp. 19-29, 1990.

[13] M. Anis and M. Elmasry, "Multi-Threshold CMOS Digital Circuits: Managing Leakage Power," Springer, 2003.

[14] Wen-Qiang Liu, Hai-Rui Wei, Leong-Chuan Kwek, "Low-Cost Fredkin Gate with Auxiliary Space," Phys. Rev. Applied 14, 054057 (2020). DOI: 10.1103/PhysRevApplied.14.054057.

[15] Yugal Kishore Maheshwari's thesis, "A Comparative Analysis for Low-voltage, Low-power, and Low-energy Flip-flops," explores the power consumption and efficiency of various flip-flops, including LLFF and TGFF.

[16] Haran Kumar G's paper, "An Efficient Low Power Adaptive Coupling Flip-Flop for Clock Gating Applications," discusses the design and power efficiency of ACFF.