A Review of GNRFET based SRAM for Low-Power Applications

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Abstract— Graphene Nanoribbon Field Effect Transistors (GNRFETs) have emerged as promising candidates for constructing low-power Static Random Access Memory (SRAM) due to their exceptional electrical properties such as high carrier mobility, low off-state leakage, and excellent scaling potential. This review explores the recent advancements in GNRFET-based SRAM designs tailored for low-power applications. Various aspects including device structures, circuit topologies, read and write operations, as well as power consumption reduction techniques are discussed. Moreover, challenges and opportunities for the widespread adoption of GNRFET-based SRAM in low-power systems are identified and analyzed. By providing a comprehensive overview of the current state-of-the-art and future prospects, this review aims to guide researchers and engineers in the development of efficient and energy-saving memory solutions for emerging technologies.

Keywords— *GNRFET, SRAM, Transistors, Cells,FinFET .*

I. INTRODUCTION

Static Random Access Memory (SRAM) plays a critical role in modern digital systems, serving as a cornerstone for on-chip memory, cache memory, and register files in processors, as well as in various other applications ranging from data buffering to high-speed data processing [1]. With the ever-increasing demand for energy-efficient electronic devices, particularly in battery-powered portable electronics, the development of low-power SRAM designs has become imperative. In this context, Graphene Nanoribbon Field Effect Transistors (GNRFETs) have attracted significant attention as promising building blocks for constructing low-power SRAM cells [2].

GNRFETs, derived from graphene, possess unique electrical properties that make them suitable for next-generation semiconductor devices. These properties include high carrier mobility, excellent mechanical flexibility, and superior scalability [3]. Moreover, GNRFETs exhibit low off-state leakage current, which is crucial for reducing static power consumption in SRAM cells, especially in standby modes.

This review focuses on examining the recent advancements in GNRFET-based SRAM designs specifically tailored for low-power applications. It begins with an overview of GNRFET device structures and fabrication techniques, highlighting their advantages over conventional CMOS-based SRAM cells [4]. Subsequently, various circuit topologies and architectures employed in GNRFET-based SRAM cells are discussed, including single-ended and differential architectures, 6T and 8T cell designs, and novel approaches for reducing write and read access times while minimizing power consumption[5].

Furthermore, the review delves into techniques for mitigating power dissipation in GNRFET-based SRAM, such as adaptive body biasing, voltage scaling, and power gating strategies. Additionally, challenges associated with GNRFET-based SRAM, such as process variability, reliability, and manufacturing costs, are addressed, along with potential solutions and future research directions[6].

By providing a comprehensive overview of the state-of-the-art in GNRFET-based SRAM for low-power applications, this review aims to serve as a valuable resource for researchers and engineers working in the field of semiconductor memory

design[7]. It identifies key opportunities and challenges in the development and integration of GNRFET-based SRAM into energy-efficient digital systems, paving the way for the realization of high-performance, low-power memory solutions for emerging technologies[8].

II. LITERATURE SURVEY

B. V. Garidepalli et al.,[1] With the evolution in the microelectronic applications like high speed processors, multimedia and in current electronic communication for artificial intelligent devices and IOT necessitates bigger SOC SRAM arrays for high performance with low power consumption and lesser space. Generally, CMOS based technology are most extensively utilized for designing of 6T SRAM cell. When the Nano scale technology is scaling down CMOS devices are usually confronting with leakage current and short channel impact. The constant scaling of CMOS technology restricts the performance of 6T SRAM cell in terms of leakage power. Leakage current is the biggest contributor in the power consumption of SRAM. So, the researchers have developed the optimistic technology using Graphene as a semi conducting channel. Graphene Nano Ribbon Field Effect Transistor (GNRFET) is a three terminal device similar to MOSFET, here the semiconducting channel is made with graphene.

S. Arora et al.,[2] Power dissipation is one of the critical considerations while designing CMOS VLSI circuits for battery- and externally-powered embedded computer applications. This work discusses a collection of methods that are well-suited for CMOS technology and are easily applicable to VLSI systems and circuit designers specifically for digital logic circuits, SRAM cells and Ternary Logic Gates. Supply-voltage-scaled CMOS is described as a low-power method for digital logic that provides a flexible design space for balancing energy (and power) consumption with circuit speed. Decoders are essential for VLSI and consideration for low power devices is in high demand as portability and battery become a challenge these days. In this work, a review of techniques and circuits used for ternary logic gates is presented. Also, decoders using GNRFET and FinFET are simulated using HSPICE Tool. Scaling traditional complementary metal-oxide semiconductors (CMOS) has been plagued by issues such as the short channel effect and leakage power. Many transistors based on FinFET, GNRFETs, and DGFETs technologies are used to improve the performance metrics like power consumption, delay, IC area etc. Also, a comparative analysis shows a reduction in power of the order of 102 with 14T and 15T GNRFET based decoder over the MOSFET counterpart.

P. K. Patel et al.,[3] presented a low-leakage graphene nano-ribbon transistors (GNRFETs)-based static random access memory (SRAM) cell in 16nm technology that operates near the sub-threshold region in this study. In comparison to conventional Si-CMOS technology, the proposed cell improves read stability and writeability by $2.67\times$ and $4.14\times$, respectively. The proposed cell considerably outperforms the existing 9T SRAMs cell in terms of power consumption, latency, read stability, and write-ability, according to the HSPICE simulation. In addition, at the low supply voltage of 325mV, the multi-threshold approach and transistor optimizations are used to improve the read static noise margin (RSNM). The proposed cell's overall power consumption is lowered by $4161\times$ when compared to a conventional 6T SRAM cell while using the multi-threshold approach in the write port. Device optimization and the multi-threshold approach, which enhances read and write performance, can considerably minimize read and write delays.

T. Hossain et al.,[4] With the advancement of technology and recent developments on Internet of Things (IoT), devices with low power and smaller size come into consideration to keep pace with the current generation's demand. Shrinking Silicon devices introduce leakage power which is inappropriate for portable devices. These limitations of silicon-CMOS transistor technology can be mitigated by new Graphene nanoribbon Field effect transistor (GNRFET) technology. GNRFET's larger on off current ratio, extremely low leakage current and low supply voltage applications makes it a perfect fit for digital applications. Static Random Access Memory (SRAM) is an integral part of a chip which consumes large amount of area and power. To accomplish current technological needs GNRFET can be used to design SRAMs for low power devices. In this work we have analysed Read Static Noise margin (RSNM), power, delays of conventioal 6T SRAM with

three other 7T SRAMs using GNRFET and results show significant improvement.

S. Joshi et al.,[5] Silicon-based Static Random Access Memory (SRAM) has not been keeping pace with technology trends due to the limited improvements in power, performance and density. This work explores graphene based SRAM as a potential replacement of silicon SRAM for future digital electronics. Due to its higher current on-to-off ratio, the graphene nanoribbon field effect transistor (GNRFET) has been considered in this work. In the nanometer regime, process variation is not only inevitable but also very pronounced. To mitigate its effects as much as possible, the Schottky-Barrier type GNRFET is considered which presents lower variation in its characteristics due to doping variation. The results show that graphene nanoribbon has a great potential in digital circuit design. The GNRFET based SRAM design presented in this work leads to significantly lower power consumption, approximately 93% compared to 45 nm silicon technology.

S. Rayeni et al.,[6] The static random access memory (SRAM) Array is used in applications such as cache memories, microprocessors, and portable devices such as smart watches and mobile phones. As technology advances to the submicron level, power dissipation becomes a major disadvantage in SRAM cells, necessitating the development of low-power applications. As a result, it's important to design a memory that consumes less power. The main motive of this work is to design 4*4, 8*8, and 16*16 SRAM array using 6T and 7T SRAM cells using Graphene Nano Ribbon Field Effect Transistor (GNRFET) technology and compare power dissipation between Complementary Metal Oxide Semiconductor (CMOS) and GNRFET technologies.

M. U. Mohammed et al.,[7] The Static Random Access Memory (SRAM) has huge impact on the overall power consumption of any digital design. SRAM consumes a significant amount of power in the idle state. Therefore, the leakage power is one of the most critical metrics in SRAM designs. This work evaluates the standby leakage power of GNRFET based 6T SRAM bitcell and compared to 10nm FinFET based 6T SRAM bitcell. It is observed that the 10nm GNRFET based SRAMs have 16.43 times less standby leakage power compared to the 10nm FinFET based SRAMs. The work also presents an analysis of the stability and reliability of GNRFET based 6T SRAM circuit with a reduced supply voltage of 500mV. The static noise margin (SNM), which is a critical measure of SRAM stability and reliability, is determined for hold, read and write operations of the 6T GNRFET SRAM cell.

P. Singh et al.,[8] In modern technologies, read stability and write ability have become major concerns in nano regime for static random access memory (SRAM) cell. This work provides the stability analysis of 6T-SRAM cell using the N-curve method. Various performance parameters namely SVNM, SINM, WTV, and WTI are evaluated for SRAM. Variation of SVNM, SINM, WTV and WTI with scaled supply voltage has been presented. A comparative analysis of CNTFET and GNRFET with conventional CMOS technology using HSPICE tool has been performed. To ensure a fair comparison of (19,0) CNTFET(D_{CNT} =1.49nm) and (13,0) GNRFET(width=1.49nm) dimensions have been chosen for proper circuit size integration.

III. CHALLENGES

Challenges in the Development of GNRFET-based SRAM for Low-Power Applications:

1. **Process Variability and Yield**: One of the primary challenges in the adoption of GNRFET-based SRAM is the inherent process variability associated with graphene-based devices. Variations in ribbon width, edge roughness, and defects can significantly impact device performance and reliability. Ensuring high manufacturing yield and consistent device characteristics pose significant challenges in large-scale production.

2. **Reliability and Stability**: Graphene nanoribbons are susceptible to environmental factors such as temperature variations, humidity, and mechanical stress, which can affect their electrical properties and long-term reliability. Ensuring the stability and robustness of GNRFET-based SRAM cells under different operating conditions is crucial for practical implementation.

3. **Integration with CMOS Technology**: Integrating GNRFET-based SRAM cells with existing CMOS

technology presents challenges in terms of process compatibility, interface compatibility, and circuit-level integration. Achieving seamless co-integration while maintaining performance, reliability, and yield requires innovative design techniques and optimization strategies.

4. **Power Consumption Reduction**: While GNRFETs offer low off-state leakage current, reducing dynamic power consumption during read and write operations remains a significant challenge. Developing efficient power management techniques, such as adaptive voltage scaling, power gating, and advanced read and write assist circuits, is essential for minimizing energy consumption without compromising performance.

5. **Signal Integrity and Crosstalk**: As device dimensions continue to shrink, signal integrity issues such as noise, crosstalk, and signal distortion become more pronounced. Maintaining signal integrity and minimizing interference between adjacent memory cells in densely packed GNRFET-based SRAM arrays require careful layout design, shielding techniques, and noise mitigation strategies.

6. **Scaling and Performance Trade-offs**: Scaling GNRFET-based SRAM to smaller technology nodes for increased density and performance often leads to trade-offs between speed, power, and reliability. Balancing these trade-offs while meeting design specifications and performance targets poses a significant challenge for memory designers.

7. **Cost and Scalability**: Despite the potential advantages of GNRFET-based SRAM, the cost of graphene synthesis, processing, and device fabrication remains relatively high compared to traditional silicon-based technologies. Achieving cost-effective fabrication processes and scalability to large-volume production are essential for commercial viability and widespread adoption.

Addressing these challenges requires interdisciplinary collaboration among material scientists, device engineers, circuit designers, and system architects. Innovative approaches in material synthesis, device fabrication, circuit design, and system integration are essential to overcome these barriers and unlock the full potential of GNRFET-based SRAM for low-power applications.

IV. GNRFET VS CMOS BASED SRAM

Comparative Study of GNRFET-based SRAM and CMOS-based SRAM for Low-Power Applications-

1. Device Technology:

- **GNRFET-based SRAM:** Utilizes graphene nanoribbon field-effect transistors (GNRFETs) as the basic building blocks. GNRFETs offer high carrier mobility, low off-state leakage, and excellent scalability potential.
- **CMOS-based SRAM:** Constructed using complementary metal-oxide-semiconductor (CMOS) technology. CMOS SRAM cells consist of six transistors (6T) typically.

2. Power Consumption:

- **GNRFET-based SRAM:** Offers potential for lower power consumption due to the inherent properties of graphene, such as low off-state leakage and high carrier mobility. Power-saving techniques like voltage scaling, power gating, and advanced assist circuits can further reduce energy consumption.
- **CMOS-based SRAM:** While CMOS SRAM cells have been optimized for power efficiency, they still exhibit significant leakage current, especially in deep submicron technologies. Techniques like power gating and voltage scaling are commonly employed to mitigate power consumption.

3. Performance:

- **GNRFET-based SRAM:** GNRFETs offer high carrier mobility, enabling faster switching speeds and potentially higher operating frequencies. However, achieving comparable access times to CMOS SRAM cells while maintaining low power consumption remains a challenge.
- **CMOS-based SRAM:** CMOS SRAM cells are well-established and offer reliable performance with fast access times. However, power constraints and limitations in scaling may hinder further improvements in performance without increasing power consumption.

4. Scaling and Integration:

- **GNRFET-based SRAM:** GNRFETs have excellent scalability potential due to the atomically thin nature

of graphene. As technology nodes continue to shrink, GNRFET-based SRAM cells can potentially achieve higher densities and integration levels.

- **CMOS-based SRAM:** CMOS scaling has been the driving force behind the continuous increase in memory density and integration levels. However, as technology nodes approach physical limits, further scaling becomes increasingly challenging due to issues such as leakage current and variability.

V. CONCLUSION

The review of GNRFET-based SRAM for low-power applications highlights the significant advancements and challenges in this emerging field of semiconductor memory design. GNRFETs offer promising characteristics such as high carrier mobility and low off-state leakage, making them attractive for constructing energy-efficient SRAM cells. Various circuit topologies, power-saving techniques, and integration strategies have been explored to exploit the potential benefits of GNRFETs in reducing power consumption and enhancing performance. The comparative study between GNRFET-based SRAM and CMOS-based SRAM reveals promising prospects and inherent challenges. GNRFET-based SRAM demonstrates potential advantages in power efficiency, scalability, and performance owing to the unique properties of graphene nanoribbons.

REFERENCES

1. B. V. Garidepalli, R. Prasad Somineni, A. Peddi and U. M. Janniekode, "Design and Analysis of 16nm GNRFET and CMOS Based Low Power 4kb SRAM Array Using 1-Bit 6T SRAM Cell," 2022 IEEE IAS Global Conference on Emerging Technologies (GlobConET), Arad, Romania, 2022, pp. 102-108, doi: 10.1109/GlobConET53749.2022.9872358.
2. S. Arora and S. L. Tripathi, "Comparative performance analysis of FinFET, CNTFET and GNRFET for low power digital logic circuit applications," 2022 IEEE International Conference of Electron Devices Society Kolkata Chapter (EDKCON), Kolkata, India, 2022, pp. 284-289, doi: 10.1109/EDKCON56221.2022.10032958.
3. P. K. Patel, M. Malik and T. K. Gupta, "Optimization Techniques for Reliable Low Leakage GNRFET-Based 9T SRAM," in IEEE Transactions on Device and Materials Reliability, vol. 22, no. 4, pp. 506-516, Dec. 2022, doi: 10.1109/TDMR.2022.3221806.
4. T. Hossain, M. S. Rahman, M. M. Rahman and A. R. A. Dibbo, "Performance Analysis of Graphene Nanoribbon Field Effect Transistor (GNRFET) based 6T and 7T SRAMs," 2020 23rd International Conference on Computer and Information Technology (ICCIT), DHAKA, Bangladesh, 2020, pp. 1-5, doi: 10.1109/ICCIT51783.2020.9392713.
5. S. Joshi, S. P. Mohanty, E. Kougianos and V. P. Yanambaka, "Graphene Nanoribbon Field Effect Transistor Based Ultra-Low Energy SRAM Design," 2016 IEEE International Symposium on Nanoelectronic and Information Systems (iNIS), Gwalior, India, 2016, pp. 76-79, doi: 10.1109/iNIS.2016.028.
6. S. Rayeni, A. Peddi, S. K. R, K. Srinivas K and P. Sai Y, "Design and Comparison of Advanced Low Power SRAM Cells using GNRFET Technology," 2021 International Conference on Communication information and Computing Technology (ICCICT), Mumbai, India, 2021, pp. 1-6, doi: 10.1109/ICCICT50803.2021.9510169.
7. M. U. Mohammed, A. Nizam, L. Ali and M. H. Chowdhury, "A Low Leakage SRAM Bitcell Design Based on MOS-Type Graphene Nano-Ribbon FET," 2019 IEEE International Symposium on Circuits and Systems (ISCAS), Sapporo, Japan, 2019, pp. 1-4, doi: 10.1109/ISCAS.2019.8702461.
8. P. Singh, R. Chandel and N. Sharma, "Stability analysis of SRAM cell using CNT and GNR field effect transistors," 2017 Tenth International Conference on Contemporary Computing (IC3), Noida, India, 2017, pp. 1-6, doi: 10.1109/IC3.2017.8284335.