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Literature Review Decimal Addition of Binary Coded Decimal

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***Abstract*— Decimal multiplication is the fundamental operation for any hardware implementation of decimal arithmetic and it is also a fundamental part to the above mentioned digital decimal-dominant applications. Many researchers suggested various techniques such as Area-Efficient and Power-Efficient Binary to BCD Converters using add 3 conversion method, High Performance FPGA-Based Floating Point Adder with Three Inputs, Decimal Multiplier on FPGA using Embedded Binary Multipliers among this the add 3 is the most frequently used method. Here in this paper an exhaustive literature review in the subject area are given.**

***Keywords*— BCD, FPGA, Arithmetic, Adder.**

I. INTRODUCTION

Decimal data processing applications have matured exponentially in modern years thereby increasing the necessity to have hardware and software support for decimal arithmetic. Decimal arithmetic is receiving noteworthy attention in marketable business and interne stand applications, providing hardware and software support in this direction is hereafter necessary calculation in saleable, scientific, and financial. Present arithmetic units are typically binary based and not decimal based. This due to the following reason: It is extremely efficient to store binary data. Utilization of binary data is very speedy on digital computers. But seeing as, decimal arithmetic is more beneficial than binary arithmetic operation; the conversion of binary data to BCD data is involved.[8].

II. LITERATURE REVIEW

In this section different author's paper are discussed -

Sri Rathan Rangisetti et.al. [1] presented four novel circuits for 7-bit Binary to BCD conversion. The first and second designs are modification of 3-3-1[1] algorithm with novel building blocks, which makes it area and delay efficient in comparison with previous design. The third circuit is the novel implementation of the shift-add algorithm that makes this design area efficient in compare with existing architectures. The final architecture presented is the implementation of the novel algorithm, which we called range detection algorithm in this paper. This range detection circuit is power efficient in comparison with existing architectures.

Simulation results specify that these shift-add and range detection designs are area-efficient and power-efficient as there is a significant decrease in area, power, and power-area product.

J. Ditmar and S. Mc Keever. [2] proposed array synthesis in system C hardware compilation : This paper discusses the mapping of arrays in a high-level system narrative to hardware.System C arrays can be mapped in two dissimilar ways inregistersMapping arrays to registers have the subsequent disadvantages**:-**

1. Take more and more logic area.
2. Less performance.
3. In FPGA"s RAM

A. Guntoro and M. Glesner. [3] proposed high performance FPGA-based floating point adder with three inputs : This paper presents the design and the achievement of an FPGA-based floating-point adder with three inputs. It can be used in Discrete Wavelet Transform (DWT) applications. The design is based on a 5-level pipeline stage in order to distribute the critical paths and to exploit the performance. The data dependencies to reduce the number of the pipeline stages and to decrease the resource allotment are examined.The design was synthesized on different FPGA devices. Other designs (Malik and IP core) were used for assessment. In terms of logic usage, it is slightly higher as compared to Malik, but still less compared to the IP core. In operating speed, it is higher than both the IP core and Malik on most of the target devices. The proposed design with the single precision, 32-bit floating-point format can be operated at 143 MHz on Xilinx Virtex2Pro - XC2VP30-7. About 19% speed gain can be achieved on Virtex2Pro and 22% on Virtex2 compared to Malik.

H. Neto and M. Vestia. [4] proposed decimal multiplier on FPGA using embedded binary multipliers: Decimal arithmetic has grown to be a primary necessity in computer arithmetic operations associated by means of human-centric applications, similar to financial and commercial, because the results should have competition exactly with those achieved by human calculations. In this work, a novel approach has come close to the introduced design of a decimal (BCD) multiplier.

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1. At first, the BDC operands are converted into binary.
2. Then the binary operands are multiplied using a 17x17 binary multiplier which is set up in most of the state-of-the-art FPGA‟s.
3. Then the binary result is converted to BCD using a narrative algorithm. The algorithm has the following two steps:-
4. The binary number is converted to a number of base-10
5. Then the base-10 binary number is converted to BCD using the typically used shift and add-3 algorithm. The proposed adder was implemented in a Xilinx Virtex 4sx35ff877 -12 FPGA. The results point toward that the proposed binary coded decimal converter is more competent than the established shift and add-3 algorithm and that the proposed decimal multiplier is very much ready for action when compared to decimal multipliers implemented with direct operation of BCD number.

S. Jang. et al. [5] proposed cache miss-aware dynamic stack allocation authors: In this author‟s work, a hardware called Dynamic Stack Allocator (DSA) is proposed to decrease cache misses by locating the stack pointer anywhere so that the cache misses probability is lowest. The proposed DSA has the subsequent components:-

Cache Miss Predictor (CMP) It adds a cache miss probability at each cache line using the narration of cache misses. When there is a cache miss, then the index of the cache line is saved in the index register and the number of cache miss is saved in the Corresponding Count register. When the register buffer is full, substitute is done by distance based LRU policy.

Stack Pointer Manager (SPM) The stack area is separating into multi sub-stacks. SPM looks up and down the buffer to identify whether indices consist of in the searching window exist or not. If searching window exists, SPM adds the consequent count value to get the total cache overlook likelihood. Then SPM energetically selects a sub-stack that has the buck cache miss probability as the stack for an application.The DSA system was employed & included by the open RISC 1200 microprocessor with 8KB direct-mapped data cache and 8KB direct-mapped instruction cache, each with 16-byte line size. In various benchmarks, it was shown that traffic among cache and main memory was decreased by DSA from 3 % to 32 %. The DSA took only 1% of the total of its core area.

Thanushkodi Praveena et al [6] proposed a unified reversible design of binary and binary coded decimal adder subtractor:-Reversible logic is one of the emerging research areas that have gained greater momentum due to the ability to produce zero power dissipation under ideal conditions.

This aspect of reversible logic circuits has found its application in various disciplines like quantum computing, nanotechnology, optical technology and low power CMOS designs. This paper presents a novel reversible logic implementation of unified Binary and BCD adder/subtractor and this single circuit proposed can perform four operations namely binary addition, binary subtraction, BCD addition and BCD subtraction based on the input given to the circuit. The circuit is compared with different BCD adder/subtractor circuits in terms of gate count, constant inputs, garbage outputs and delay.

Emre Salman.et al. [7] proposed a design of efficient reversible BCD adder–subtractor architecture and its optimization using carry skip logic: In the present era, reversible logic designs play a very critical role in nanotechnology, low power complementary metal-oxide semiconductor (CMOS) designs, optical computing and, especially, in quantum computing. High power dissipation and leakage current in deep submicron technologies is a severe threat in applications created today. As a consequence, design of data path elements in reversible logic has gained much importance. In this study, a novel design of binary coded decimal (BCD) adder/subtractor in reversible logic has been proposed. As a further optimization of the proposed reversible decimal design, Carry Skip Adder (CSK) logic is used for reversible ripple carry adder stages. This reduces delay but at the expense of little hardware. The proposed BCD adder/subtractor and its optimized version are designed using structural VHDL and simulated using ModelSim 6.3f. Performance analysis reveals that the proposed BCD design demonstrates reductions in gate count, garbage outputs and constant inputs of 30.5%, 46% and 28%, respectively, and its optimized version exhibits 19.4%, 32.4% and 16% reductions in gate count, garbage outputs and constant inputs compared to the design.

Ashis Kumer Biswas et al. [8] proposed efficient approaches for designing reversible binary coded decimal adders. Reversible logic has become one of the most promising research areas in the past few decades and has found its applications in several technologies; such as low-power CMOS, nano computing and optical computing. This paper presents improved and efficient reversible logic implementations for Binary Coded Decimal (BCD) adder as well as carry skip BCD adder. It has been shown that the modified designs outperform the existing ones in terms of number of gates, number of garbage outputs, delay, and quantum cost. In order to show the efficiency of the proposed designs, lower bounds of the reversible BCD adders in terms of gates and garbage outputs are proposed as well.

AK Biswas et al. [9] proposed a reversible logic that has become one of the most promising research areas in the past few decades and has found its applications in several technologies; such as low power CMOS, nano computing and optical computing. This paper presents improved and efficient reversible logic implementations for Binary Coded Decimal (BCD) adder as well as carry skip BCD adder. It has been shown that the modified designs outperform the existing ones in terms of number of gates, number of garbage output and delay.

M Islam et al. [10] proposed reversible circuits have applications in digital signal processing, computer graphics, quantum computation and cryptography. In this paper, a generalized k* k reversible gate family is proposed and a 3*3 gate of the family is discussed. Inverter, AND, OR, NAND, NOR, and EXOR gates can be realized by this gate. Implementation of a full-adder circuit using two such 3* 3 gates is given. This full-adder circuit contains only two reversible gates and produces no extra garbage outputs.

Hafiz Md Hasan Babu et al. [11] proposed reversible logic synthesis for minimization of full-adder circuit: Reversible logic is of the growing importance to many future technologies. A reversible circuit maps each output vector, into a unique input vector, and vice versa. This paper introduces an approach to synthesis the generalized multi-rail reversible cascades with minimizing the "garbage bit" and number of reversible gates, which is the main challenge of reversible logic synthesis. This proposed full-adder circuit contains only three gates and two garbage outputs whereas earlier full-adder circuit. [11]

Bayrakci and Ahmet Akkas. [12] proposed BCD adder with efficient carry generation in which the proposed BCD adder with efficient carry generation using analyzer circuit performs well in terms of delay compared to architectures mentioned in literature and shows better area performance.

Anshul Singh et al.[13] proposed a novel architecture for BCD addition and subtraction designed a novel architecture for BCD addition and subtraction. The design uses three major blocks viz., PG block, prefix block and the correction block and generates carry without any extra logic thus performing better in terms of area performance compared to the BCD adder in (Veeramachaneni et al 2008).

Chetan Kumar et al.[14]proposed a unified architecture for BCD and binary addition and presented a unified architecture for BCD and binary addition. Though the circuit has lower delay compared to the architectures mentioned in literature the design of post correction circuitry poses problems for multi-bit operands.

Sundaresan et al .[15]proposed a pioneer work on design of reduced delay BCD adder using Carry Look Ahead (CLA) in which a pioneer work on design of reduced delay BCD adder using Carry Look Ahead (CLA) Adder in the initial stage being followed by carry network and correction logic in the second and third stages. Though the circuit is fast compared to the architecture in (Chetankumar et al 2011), the use of CLA adder in the initial stage increases area cost.

Al-khaleel et al . [16] proposed a correction free BCD adder in which the input operands are split and added in two stages. Stage 1 adds the most significant three bits of a four bit BCD number and its result is passed to stage 2 and added with the LSB. The latency of the architecture is very less compared to the conventional and Thapliyal et al (2006) architectures.

C. Sundaresan et al. [17] proposed an arithmetic and memory address computation is performed using adder operations. Hence, design of adders form an important subset of electronic chip design functionality. Performance of BCD adders is to be considered with gate count, area, delay, power consumption. A new BCD adder design is attempted here to reduce the delay and thereby increasing the speed of response. BCD adder design is considered with respect to high speed addition requirement including multi operand addition, multiplication and division. The new architecture supports 64 bit and 128 bit operands and reduces the delay by adding parallelism.

H R Bhagyalakshmi et al. [18] proposed a reversible logic which is very essential for the construction of low power, low loss computational structures which are very essential for the construction of arithmetic circuits used in quantum computation, nano technology and other low power digital circuits. In the present paper an optimized and low quantum cost one digit BCD adder and an optimized one digit carry skip BCD adder using new reversible logic gates are proposed. The proposed work is best compared to the other existing circuits.

MILOSˇ D. ERCEGOVAC et al. [19] proposed a radix-r digit-recurrence algorithm for complex square-root. The operand is rescaled to allow the selection of square-root digits by rounding of the residual. This leads to a simple hardware implementation of digit selection. Moreover, the use of digit recurrence approach allows correct rounding of the result if needed. The algorithm, compatible with the complex division presented in Ercegovac and Muller (BComplex Division with Prescaling of the Operands,^ in Proc. Application-Specific Systems, Architectures, and Processors (ASAP_03), The Hague, The Netherlands, June 24–26, 2003), and its design are described.

We also give rough estimates of its latency and cost with respect to implementation based on standard floating-point instructions as used in software routines for complex square root.

Rishabh Panday et al. [20] in the present days after increasing the complexity in the computation, internet based applications we need a fast and compact decimal adder which work with less delay and same power consumptions. So we can design a pipelined four input decimal adder using the DG, DP signals and correction digits. By using the CSA, CLA, PG generator and with a register they reduced the delay of the adder with 46.22% comparison to conventional decimal adders by synthesize the simulation in Xilinx software. In their proposed work decimal adder is divided in two parts and a register is used in between that for reduce the delay of critical path. So the pipelined decimal adder can work fast addition of the decimal numbers.

T.J Sunil Daya Sagar et al.[21] presented a new architecture for a Binary to BCD converter which forms the core of our proposed high speed decimal multi-operand adder. Our proposed design contains various improvements over existing architectures. These include an improved BD Converter that helps in reducing the delay of the multi-operand decimal Adder. Simulation results indicate that with a marginal increase in area, the proposed BD converter exhibits an improvement in delay over earlier designs. Further the decimal multi-operand adder achieves faster design when compared to previously published results.

ME Students et al. [22] proposed the core of every microprocessor, digital signal processor (DSP), and data processing application-specific integrated circuit(ASIC) is its data path. At the hearts of data paths and addressing units are arithmetic units, such as a comparators, adders, and multipliers. In this paper, a 4-input decimal adder has been developed using 90 nm CMOS technology. The schematic of decimal adder is designed and simulated for its behavior using DSCH-3.1 The layout of simulated adder is created using Verilog based net list file which is further simulated using Microwind 3.1 to analyze the performance. The result shows that designed decimal adder has consumed 0.603mW power.

Michael F. Cowlishaw et al. [23] proposed a decimal arithmetic that is the norm in human calculations, and human-centric applications must use a decimal floating-point arithmetic to achieve the same results. Initial benchmarks indicate that some applications spend 50% to 90% of their time in decimal processing, because software decimal arithmetic suffers a 100× to 1000× performance penalty over hardware.

The need for decimal floating-point in hardware is urgent. Existing designs, however, either fail to conform to modern standards or are incompatible with the established rules of decimal arithmetic. This paper introduces a new approach to decimal floating-point which not only provides the strict results which are necessary for commercial applications but also meets the constraints and requirements of the IEEE 854 standard. A hardware implementation of this arithmetic is in development, and it is expected that this will significantly accelerate a wide variety of applications.

Mark A. Erle et al. [24] proposed a decimal multiplication is important in many commercial applications including financial analysis, banking, tax calculation, currency conversion, insurance, and accounting. This paper presents the design of a decimal floating-point multiplier that complies with specifications for decimal multiplication given in the draft revision of the IEEE 754 standard for floating-point arithmetic (IEEE 754R). This multiplier extends a previously published decimal fixed point multiplier design by adding several features including exponent generation, sticky bit generation, shifting of the intermediate product, rounding, and exception detection and handling. The core of the decimal multiplication algorithm is an iterative scheme of partial product accumulation employing decimal carry-save addition to reduce the critical path delay. Novel features of the proposed multiplier include support for decimal floating- point numbers, on-the- fly generation of the sticky bit, early estimation of the shift amount, and efficient decimal rounding. Area and delay estimates are provided for a verified Verilog register transfer level model of the multiplier.

Himanshu Thapliyal, et al. [25] proposed an IEEE 754r which is the ongoing revision to the IEEE 754 floating point standard and a major enhancement to the standard is the addition of decimal format. This paper proposes two novel BCD adders called carry skip and carry look-ahead BCD adders respectively. Furthermore, in the recent years, reversible logic has emerged as a promising technology having its applications in low power CMOS, quantum computing, nanotechnology, and optical computing. It is not possible to realize quantum computing without reversible logic. Thus, this paper also paper provides the reversible logic implementation of the conventional BCD adder as the well as the proposed carry skip BCD adder using a recently proposed TSG gate.

Jeff Rebacz et al. [26] proposed a decimal arithmetic is desirable for high precision requirements of many financial, industrial and scientific applications.

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Furthermore, hardware support for decimal arithmetic has gained momentum with IEEE 754- 2008, which standardized decimal floating-point. This paper presents a new architecture for two operand and multi-operand signed-digit decimal addition. Signed-digit architectures are advantageous because there are no carry-propagate chains. The proposed signed-digit adder reduces the critical path delay by parallelizing the correction stage inherent to decimal addition. For performance evaluation, we synthesize and compare multiple unsigned and signed-digit multi-operand decimal adder architectures on 0.18 µm CMOS VLSI technology.

III. Problem Statement

Decimal Arithmetic is widely utilized as a part of web based applications, commercial and budgetary purposes .Therefore the hardware that can support decimal arithmetic is turning into a need. The determination for the decimal balanced point algorithm were integrated which is very slow process, complex and posses more area. These are executed using iterative methods or look up table based reduction technique. The inspiration behind BCD architecture enhancing is to expand their efficiency in expression of their speed and computational routine. In this thesis we have introduced an algorithm called shifting and adding by 3 algorithms that makes it area efficient over existing architecture of previous paper.

Table: 2.1
Literature Review

Paper	Power D nW)	lay (nS)	Year	BIT	Application
Multi-operand Parallel Decimal Adder: A Mixed Binary and BCD Approach	0.120	0.4120	2007	8 bit	Dedicated hardware for decimal floating point arithmetic is becoming a necessity in commercial and financial applications which demand high speed decimal computation. Multi-operand decimal addition is the core of other arithmetic operations.
Improving the Speed of Parallel Decimal Multiplication	0.1508	0.4723	2009	7 bit	Computations in commercial, scientific, financial, and Internet-based computer applications.
A parallel decimal adder with carry orrection during binary accumulation	0.33	0.2410	2012	16 OPE RAN D	Conversion requires a relatively small and can afford fast operation
Decimal / Binary Multi-operand Addeing a Fast Binary to Decimal Converter	0.37	0.2617	2014	7 bit	BCD designs with low power for zee BEE receiver and wireless sense network But there is no sample and holdcircuit
Proposed Thesis	0.42	0.2710	2016	16 bit	Decimal Arithmetic is receiving noteworthy attention in marketable business and internet stand Applications, providing hardware and software support in this direction is hereafter necessary calculation in saleable, scientific and financial.

Table 1 shows the work done on adders in the consecutive years and the comparison of results with the proposed thesis in terms of power, delay and respective application.

IV. Conclusion

This paper we read so many paper related to BCD adder and adder. We found by study that Decimal Arithmetic is receiving noteworthy attention in marketable business and internet stand Applications, providing hardware and software support in this direction is hereafter necessary calculation in saleable,scientific and financial.

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