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VLSI Based High Speed Parallel FIR Filter Design

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***Abstract*— New parallel FIR filter is designed based on advantageous polyphase decomposition. Based on this algorithm, the number of multipliers in the sub filter section gets reduced by the addition of adders. The reduction of multipliers increases with increase in length of the filter but addition of adders remains fixed even if the length of the filter increases. This algorithm first derives smaller length fast parallel filters and then cascaded to design parallel FIR filters of larger block size. The performance of parallel FIR filters structure based on carry save adder and Constant multiplier explained.**

***Keywords*—Fast Finite Impulse Response (FIR); Fast FIR Algorithm (FFA); Digital Signal Processing (DSP); Very Large Integration (VLSI).**

I. INTRODUCTION

Parallel processing in DSP is a technique to use different tasks simultaneously. Due to characteristics of parallel processing, the parallel Digital Signal Processing design frequently has N number of outputs, resulting in higher throughput than not parallel. In a parallel system, the sampling time is not equal to the clock time. Parallel processing can reduce the power consumption of a system by reducing the supply voltage. The design of a digital filter is a difficult task. The output of a system can be determined by convoluting its input signal with the impulse response. The recent way of designing a FIR filter is by determining filter based on filtering algorithms. It is totally based upon fixing the length of the filter. The basic step in determining the algorithm is poly phase decomposition in which small length filter is derived and by iterating those structures to form larger blocks.

II.BACKGROUND WORKS

To reduce the computational complexity of digital filters block processing concept is generalized by the systems. Various algorithms that are used for implementing filter structure are as follows: Based on Iterated Short Convolution Algorithm (ISCA) which is a mixture of Mixed Radix Algorithm (MAD) and fast convolution algorithm which is used to design hardware efficient Finite Impulse Response (FIR) filter [3]. Block filter quantization algorithm is implemented in order to reduce the hardware cost. Delay Element Matrix (DEM) is used to reduce the number of multiplication and addition by adding delay element [5] .Another method to reduce hardware complexity is by transforming the filter structure into linear convolution and then implementing Iterated Short Convolution Algorithm (ISCA) [4]. In order to reduce the chip size and integrate multichip solution into single chip, it is necessary to limit the silicon area. This produces FIR filter with reduced hardware. This paper is organised as follows. The Fast FIR Algorithm is explained in section III. The Existing work is given in section IV. The proposed FFA structure is given in section V. The Section VI explains about the Results and Discussions. Section VII explains the conclusion.

III. ALGORITHM

The FFA algorithm is derived from advantageous polyphase decomposition. The polyphase decomposition can be formulated as follows:

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$$y(n) = h(n) * x(n) = \sum_{i=0}^{N-1} h(i)\, x(n-i), \quad n = 0,1,2... \quad (1)$$

Where {x (n)} is input sequence, {h (n)} is filter coefficients.

$$Y(z) = H(z).X(z) = \left(\sum_{n=0}^{N-1} h(n)\, z^{-n}\right)\left(\sum_{n=0}^{N-1} x(n)\, z^{-n}\right) \quad ...(2)$$

The input sequence x (n) is decomposed into odd and even parts as

$$X(z) = x(0) + x(1)\, z^{-1} + x(2)\, z^{-2} + ... \quad (3)$$

$$= [x(0) + x(2)\, z^{-2} + x(4)\, z^{-4} + ...] + z^{-1}\,[x(1) + x(3)\, z^{-2} + x(5)\, z^{-4} + ..] \quad (4)$$

The Z-transform of the sequence x (n) can be expressed as,

$$X_0(Z^2) + Z^{-1} X_1(Z^2) \quad (5)$$

Similarly, we can expressed as,

$$H_0(Z^2) + Z^{-1} H_1(Z^2) \quad (6)$$

$$Y_0(Z^2) + Z^{-1} Y_1(Z^2) \quad (7)$$

$X_0(Z^2)$ & $X_1(Z^2)$ are the z-transforms of x (2k) and x (2k+1).

$$Y_0(Z^2) = X_0(Z^2)\, H_0(Z^2) + Z^{-2}[X_1(Z^2)\, H_1(Z^2)] \quad (8)$$

$$Y_1(Z^2) = X_0(Z^2)\, H_1(Z^2) + X_1(Z^2)\, H_0(Z^2) \quad (9)$$

The above equation represents output of two parallel filter. In the similar way we can derive expression for filters of higher taps.

The parallel FIR filter can be derived from polyphase decomposition as

$$\sum_{P=0}^{L-1} Y_p(Z^L) Z^{-P} = \sum_{q=0}^{L-1} X_q(Z^L) Z^{-q} \sum_{r=0}^{L-1} H_r(Z^L) Z^{-r} \quad (10)$$

From this filtering equations can be derived as

$$X_l = \sum_{i=o}^{\infty} z^{-k}\, x(LK + l), l = 0,1,2..L-1 \quad (11)$$

$$H_m = \sum_{m=o}^{\infty} z^{-k}\, h(LK + m), m = 0,1,2..L-1 \quad (12)$$

$$Y_n = \sum_{n=o}^{\infty} z^{-k}\, y(LK + n), \; n = 0,1,2..L-1 \quad (13)$$

By using these equations the parallel filter is designed for filter of any length. The higher length filters are derived by cascading or iterating filters of small length.

IV. Existing System

2 x 2 FFA (L=2)

The two parallel filters can be implemented using Fast FIR Algorithm as,

$$Y_0 = H_0 X_0 + Z^{-2} H_1 X_1 \quad (14)$$

$$Y_1 = (H_0 + H_1)(X_0 + X_1) - H_0 X_0 - H_1 X_1 \quad (15)$$

The system design diagram of the two parallel FIR filter is obtained by the output equation Y_0 and Y_1.The design will require three FIR sub filter sections, one preprocessing and three post processing adders.

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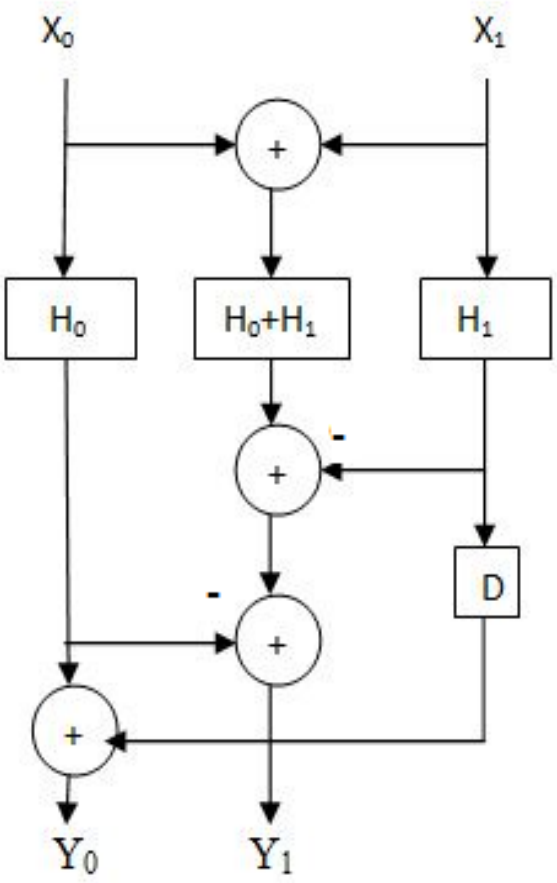

Fig.1. Two parallel FIR filter using FFA

V.PROPOSED SYSTEM

2 x 2 Proposed FFA

$$Y_0 = \left\{0.5\left[\begin{matrix}(H_0 + H_1)(X_0 + X_1) + (H_0 - H_1) \\ (X_0 - X_1)\end{matrix}\right] - H_1X_1\right\} +$$

$$Z^{-2}H_1X_1 \qquad (16)$$

$$Y_1 = \{0.5[(H_0 + H_1)(X_0 + X_1) - (H_0 - H_1)(X_0 - X_1)]\} \qquad (17)$$

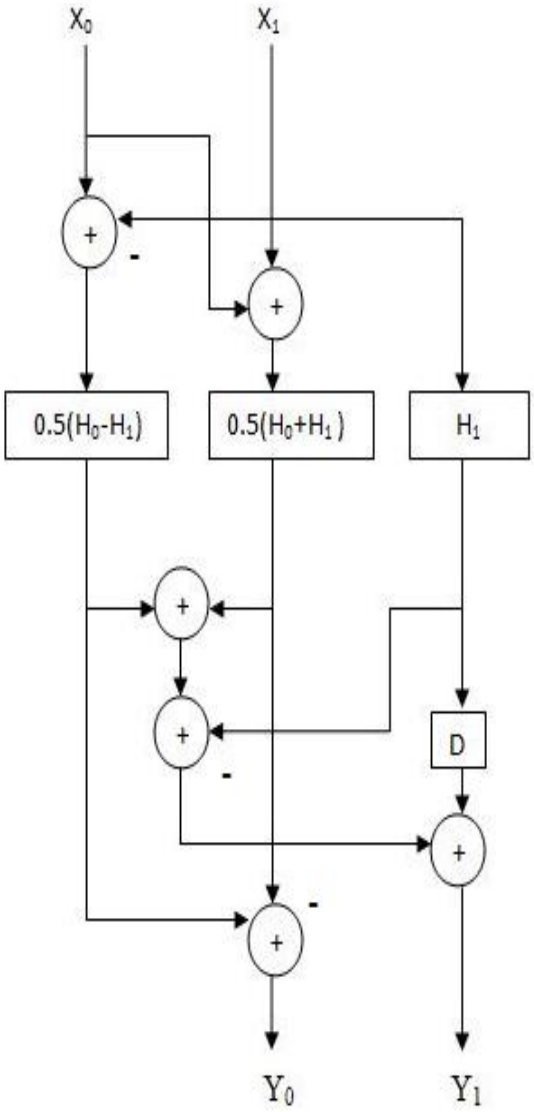

Fig.2. Proposed three parallel FIR filter using new FFA

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Using symmetric coefficients, it can earn one more symmetric coefficient sub filter blocks and also it allows reusing of multiplication operation of total number of taps. Using carry save adder and constant multiplier in the proposed design, enables the fast operation.

A. Carry Save Adder

It is a high speed multi operand adder using for fast arithmetic operation. It is implemented by standalone full adders. Carry save adder of N bit designed using N bit full adder. It computes sum and carry based on input numbers.

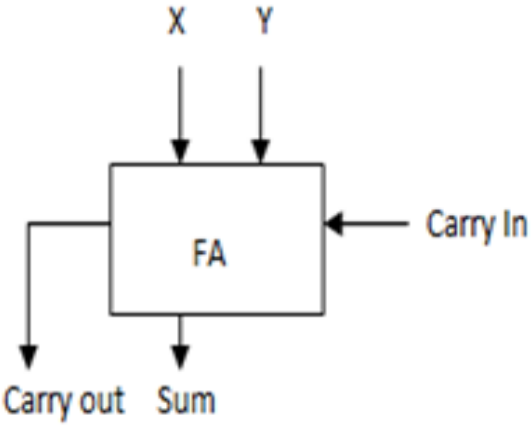

Fig.3.Carry Save Adder

B. Constant Multiplier

Multiplication using Constant is commonly used for filter design in Digital Signal Processing circuits. Here we can perform multiplications based on shift-and-operation. Adders, shifts are used in the place of general multiplier.

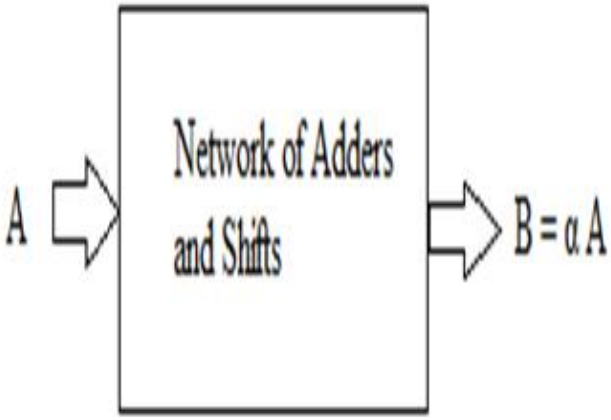

Fig.4.Constant Multiplier

VI.RESULTS AND DISCUSSION

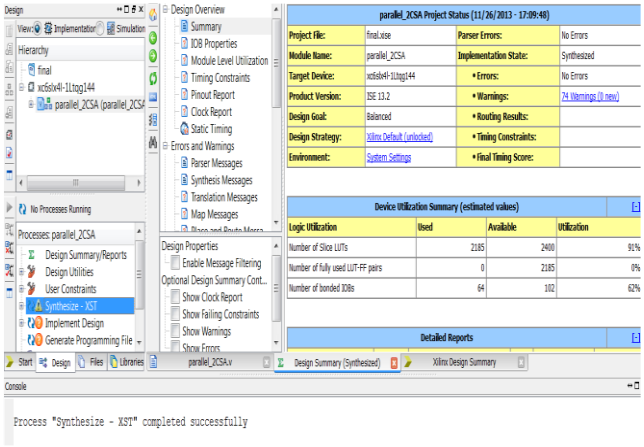

Fig.5. Design Summary of VLSI Based High Speed Parallel FIR Filter

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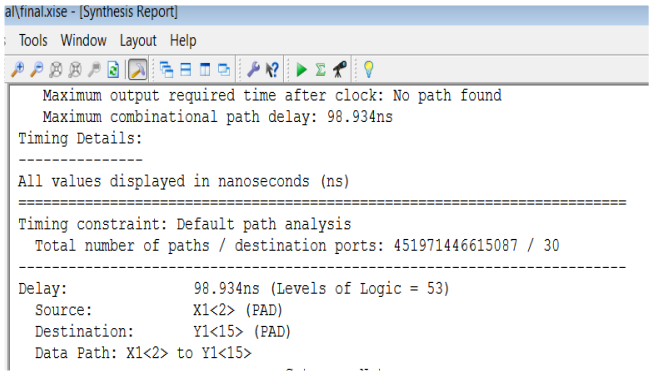

Fig.6. Delay Analysis of FIR Filter

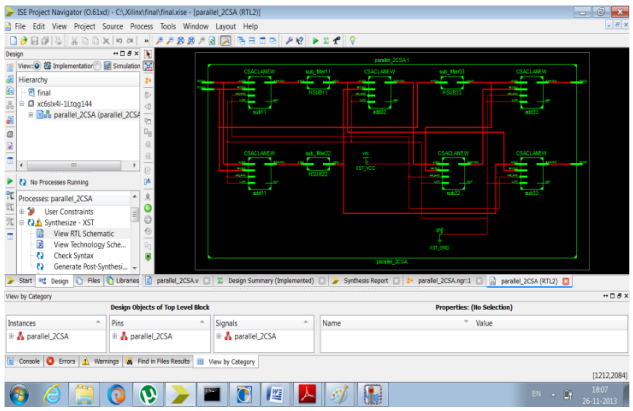

Fig.7. Schematic of Two Parallel FIR Filter

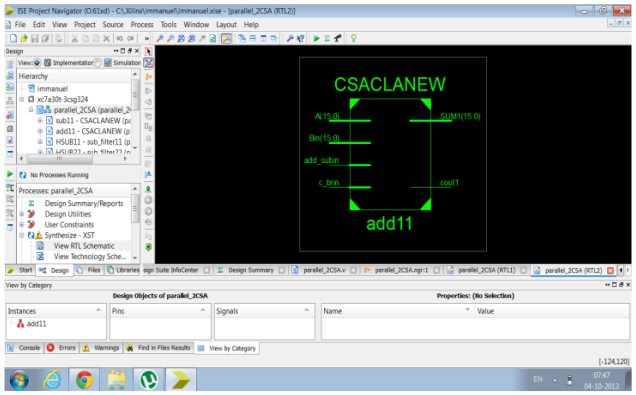

Fig.8. Schematic of Carry Save Adder

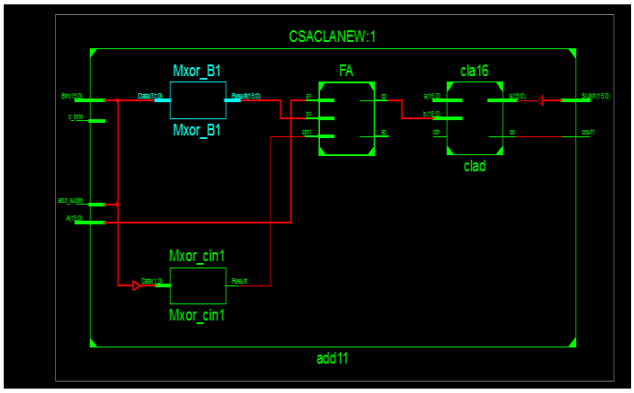

Fig.9. Detailed Schematic of Carry Save Adder

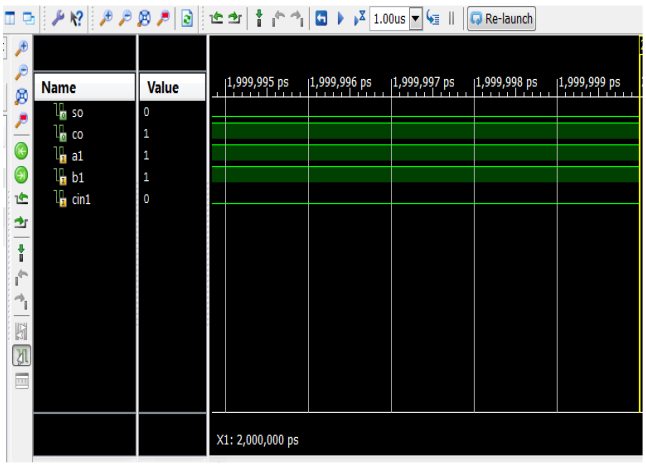

Fig.10. Simulation of 1 Bit Full Adder

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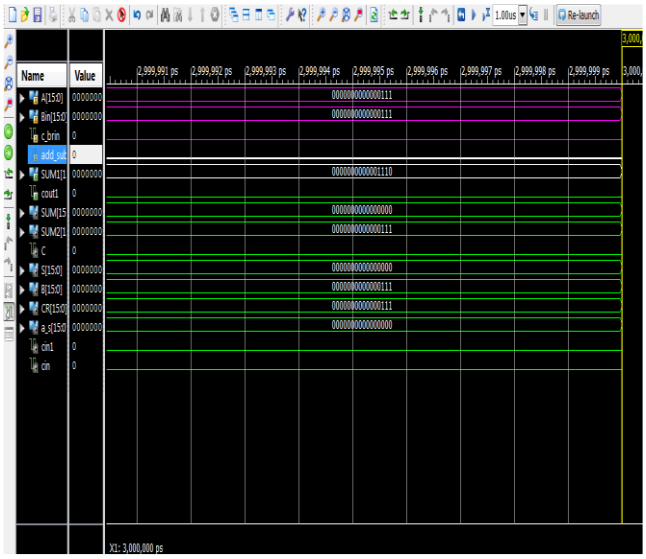

Fig.11. Simulation of 16 Bit Carry Save Adder

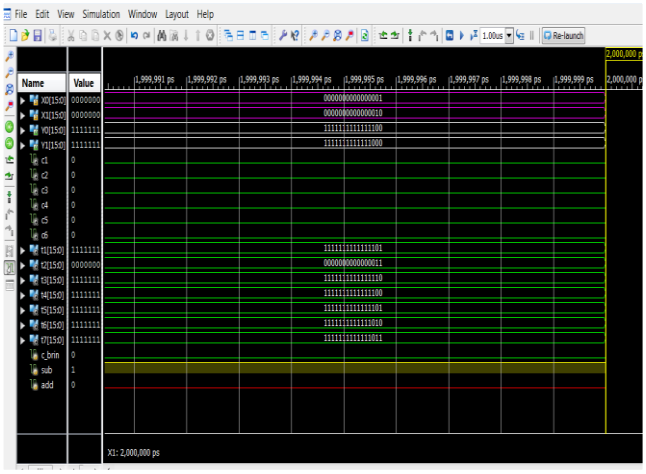

Fig.12. Simulation of 16 bit Two Parallel FIR Filter

Fig.5 explains the summary of the design of two parallel FIR filter. Fig.6.explain about the delay analysis of FIR filter, here we using combinational circuit so no clock is needed to provide. it is a overall delay in circuit operation. Fig.7 explains the schematic of 16 bit two parallel FIR filter.

Fig.8 explains the schematic of 16 bit carry save adder which is called for designing FIR filter. Fig.9 explains the detailed schematic of the components used to design the carry save adder. Fig.10 explains simulation of 1 bit full adder using Xilinx ISIM simulator. Fig.11 explains the simulation of 16 bit carry save adder. Fig.12 explains the simulation of 16 tap two parallel FIR filter using carry save adder and constant multiplier.

VII. Conclusion

Multipliers are the major portions in hardware consumption for the parallel FIR filter implementation. The proposed structure explains about the nature of even symmetric coefficients and save a significant amount of multipliers at the expense of additional adders. The number of increased adders stays still when the length of FIR filter becomes high, when the number reduction of multipliers increases along with the length of FIR filter. Advantageous poly-phase decomposition with symmetric convolution is used which is better than the existing FFA structure. Here we used Carry save adder and constant multiplier which lead minimum delay of operation.

VIII. References

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