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A Review on Performance of Comparator in Analog to Digital Converter

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Abstract: **- The analog to digital converters is the lock devices in current era of electronic items. As the digital signal executing industry steps up the ADC structure becomes high and high target for scientists. Now days an ADC becomes an instance of the system on IC board at place of standalone circuit for signal converters. This increases the needs on ADC structure concerning for sample speed, power, area, resolution, disturbance etc. New ideas and methods are moving to generate as day by day pass to get high performance ADCs. So, it is said that the comparators are the lock analog building mode of any flash ADC and highly influence performance. A high degree of comparator accuracy is essential for best ADC performance. In this paper we discuss on recently observation on comparator deployed in analog to digital convertor and also observe the performance of ADC by using this comparator.**

Keyword: **Comparator, low power, high speed, low area**

I. INTRODUCTION

The signals in the real way are analog as like light, sound, etc. In a way to digitally process any analog signal we require to transform the analog signal into digital form by following a circuit diagram called analog-to-digital converter. The process of a comparator is to produce an output voltage, which is high or low based on whether the amplitude of the given input is higher or lower than a linked signal. It generates a binary output whose value is depended on a matching of two analog given inputs. Typical comparators have variation type of structure, and they can be further categorized into open-loop and dynamic comparators. The open-loop comparators are functionally operational amplifier [1]. Dynamic comparators use positive feedback common to flip-flops to accomplish the matching of the magnitude between input and the external linked signal. However these variation types of comparator are intrinsically typically in structure and utilize high amount of power. On the other way, single ended comparator structure may be inserted as an analog comparator at place of using a whole analog block of comparator.

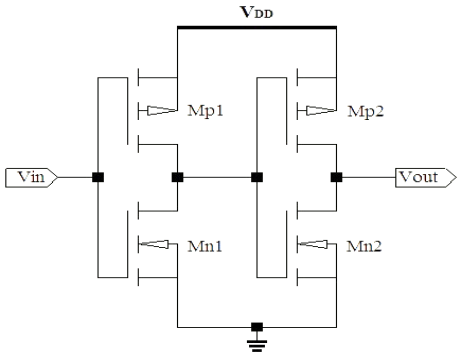

Figure 3: Functional circuit of a comparator

II. ANALOG TO DIGITAL CONVERTER

Analog to digital converters are the generally building modes that offer an interface between an analog empire which consider only an analog value (voltage/current) and transform it into digital form that can be executed by a microprocessor. The output is continuing of digital values that have transformed a continuous time and continuous-amplitude analog signal to a discrete time and discrete-amplitude digital signal.

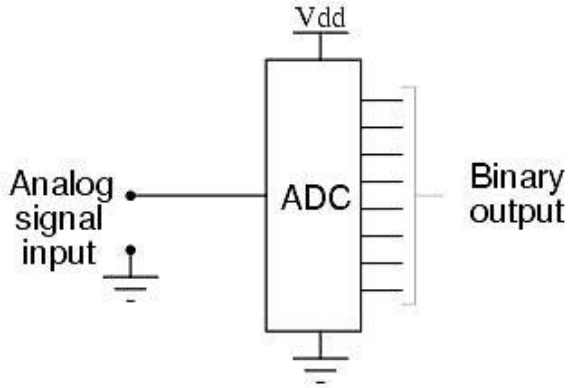

Figure 2: Connecting components of ADC [2]

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The flash ADC works at very rapid speed with lower resolution. It is also known a parallel ADC due to its parallel execution.

III. LITRETURE SURVEY

In a way to step down the power utilization and enhance the performance matrices of ADC, the scientist generally target on the optimization of the comparator circuit. Under this heading, the research work under discussion considers ADC structure using threshold voltage scaling of the comparator.

In the year 2011, all categories of ADCs the ADC are not only popular for its signal conversion rate but also it becomes the instance of other categories of ADC as an example pipeline and multi bit Sigma Delta ADCs. The main issue with an ADC is its power utilization, which steps up in number of bits. The performance selecting blocks in such ADCs are generally comparators. This research work compares the power utilization of different comparators used in flash ADCs with CMOS method [3].

In the year 2012, they model a pipelined flash Analog-to- Digital Converter (ADC) to get rapid speed using 0.18umCMOS component. The results gained are also displayed here. The physical design is more compact than the recent model. Power, processing time, and area are all step down. This model can be deployed for modem high speed ADC applications [4].

In the year 2013, the performance of Flash Analog-to-Digital converter is highly influenced by the selection of Comparator and Thermometer to Binary encoder model. The work examines the model and pre-simulation of a , 3bit and an 4bit analog to digital converter for low power CMOS. It needs 2N-1 comparators, an encoder to convert thermometer code to binary code. The model is simulated in cadence environment using specter simulator under 90nm technology. The pre simulation outputs for the model represents a low power dissipation of 87uw for the comparator and 1.05mW and 1.984mW power dissipation for 3-bit and 4-bit Flash ADC respectively. The circuit executes with an input frequency of 25MHz and 1.5V supply with a transform time of 2.162ns and 6.182ns for 3-bit and 4-bit ADC respectively. [5]

In April, 2014, the main demerit of flash type ADC is power hungry so the target is to model a low power ADC with low power comparator. The model facts are belonged to obtain, phase, gain bandwidth, resolution, speed, and area and power utilization. Simple two stage op-amp with miller capacitance can be used as a high gain comparator. It can be easily executed at low power. It is implemented in 180nm technology using cadence virtuoso analog design environment simulation. The op-amp uses a 1.8volt Vdd and a -1.8volt Vss and utilizes a power of around 0.9mW (as per post layout simulations). The analog output of each comparator is encoded using cascading full adder modeled by pass transistor logic that makes the circuit rapid [6]. In the month of May of year 2014, Watt feature of various CMOS comparators is displayed. Topologies examined are two modes OPAMP, clock driven preamplifier-latch and rapid speed differential clocked comparator. These topologies are implemented in many methods such as 0.18, 0.25, 0.35µm using Mentor Graphics [7]. Then in the June month of year 2014, by using the new VSV comparator, the modeled 6-bit Flash ADC exhibits significant enhancement in terms of power and speed of recently reported Flash ADCs. The implementation result display that the converter utilize peak power 2.1 mW from a 1.2 V supply and get the speed of 1 GHz in a 65nm standard CMOS method [8].

The Flash ADC is the Fast ADC. For modeling the ADC, the parameters nessicty are Static and Dynamic. In static parameters Differential Non Linearity Error (DNLE), Integral Non Linearity Error (INLE) and in dynamic parameters Signal to Noise Ratio (SNR), Effective Number of Bits (EONB), Spurious-Free Dynamic Range (SFDR), Dynamic Range (DR). The model generates which include first CMOS inverter used in CDC structure, MUX deepened Decoder and DAC [9].

IV. COMPARISON

The following table describes the comparison in between the existed comparator on basis of their performance.

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Table I:
Comparison Summary

Parameter	Year 2011	Year 2012	Year 2013	Year 2014	Year 2015
Resolution	6-bit	6-bit	6-bit	6-bit	6-bit
Architecture	Flash	Flash	Flash	Flash	Flash
Technology	65 nm	90 nm	130 nm	65 nm	250 nm
DNL (LSB)	0.3	0.5	0.4	0.5	-
INL (LSB)	0.6	0.96	0.6	0.5	-
Voltage Supply	1.2 V	0.9 V	1.2 V	1.2 V	2.5 V
Power Dissipation	2.1 mW	98 mW	90 mW	12 mW	66.8 mW
Samples/sec.	1G	3.5G	600M	800M	1G
Ladder Network	No	Yes	Yes	Yes	No

V. CONCLUSION

During the study of high speed comparator we filtered out some comparison. To solve this comparison, hence the worst case input signal frequency is nyquist frequency therefore the only selecting factor to select nearly resistance value is coupling capacitance of the comparator. When the number of bits steps up then the capacitance at the input of comparator mode improve as well and if we take the obstruction value fix for improving number of bits then the linked value will vary due to kickback disturbance of noise and if the sampling speed is high enough then the comparator match wrong given inputs and this will steps down the overall output of the design.

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