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Simulation of Interleaved Buck Converter Fed PMBLDC Drive System with Input Disturbance

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***Abstract*— This paper proposes an interleaved buck converter (IBC) with input disturbance to feed a low voltage Permanent Magnet Brushless DC Motor (PMBLDC) drive. PMBLDC is one of the best electrical drives that have increasing popularity, due to their high efficiency, reliability, good dynamic response and very low maintenance. This makes the interest of simulating an ideal PMBLDC motor and its associated Drive System. In this work an IBC is used to control the PMBLDC motor. It has three active switches which are connected in series and a coupling capacitor is employed in the power path. It has the advantages of low switching losses, improved step down conversion ratio, higher efficiency, higher switching frequency, low inductor power loss and reduced ripple current. A disturbance circuit is introduced in the input stage of the interleaved buck converter, which analysis the performance of the PMBLDC at variations in the input. The simulation of the interleaved buck converter fed PMBLDC motor drive system with input disturbance circuit is done using the software package MATLAB/SIMULINK. The features, operation and simulation results of the IBC fed PMBLDC drive system with input disturbance results are presented in this paper to verify the theoretical analysis.**

***Keywords* — Interleaved Buck Converter, disturbance circuit, low voltage stress, PMBLDC Motor.**

I. INTRODUCTION

Permanent magnet brushless DC (BLDC) motor is highly used in automotive, industrial, and household products because of its high efficiency, high torque, ease of control, and lower maintenance [2], [4]. BLDC motor has better speed torque characteristics and current torque characteristics and these can be controlled very easily. A BLDC motor is designed to utilize the trapezoidal back EMF with square wave currents to generate the constant torque.

A conventional BLDC motor drive is generally implemented via a six-switch, three phase inverter [5] and three Hall-effect position sensors that provide six commutation points for each electrical cycle. Cost minimization is the key factor in fractional horse-power BLDC motor drive for Home applications. It is usually achieved by elimination of the drive components such as power switches and sensors. Therefore effective algorithms should be designed for the desired performance and the relevant drive system which in turn controls the motor for all its defined applications with high efficiency, as well as good in maintaining the speed for variable torque. Mathematical modeling of DC to DC converters is given by Luo [1 & 3]. Efficient Modelling of PMBLDC is given by Lee [4]. PID control of brushless motor is given by Othman [6], Four Switch / Reduced Switch Converters are given by Lee [8]. By using Interleaved Buck Converter high power factor can be maintained, which is given by J.Marcos Alonso [10]. Then Interleaved Buck Converter having Low Switching Losses and Improved Step-Down Conversion ratio is discussed by Il-Oun Lee [11]. The above literature does not deal with IBC fed PMBLDC drive system with input disturbance circuit. This work proposes IBC for the control of PMBLDC Drive Systems input voltage distribution.

II. INTERLEAVED BUCK CONVERTER FED PMBLDC MOTOR DRIVE

Depending upon the motor load, the motor input voltage should be maintained constant whatever may be the load condition. So a buck converter fed PMBLDC motor drive system is used. Now to have further more advancement and efficient drive system, we are going to use interleaved buck converter system [9] fed PMBLDC drive system.

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Mainly the PMBLDC drive system requires non-isolation and a good step down conversion ratio at high output current with low ripples. This makes the attention of Interleaved Buck Converter fed PMBLDC drive system [13]. The semiconductor devices used has high voltage rated devices, which in turn has poor characteristics such as high cost, high on resistance, high forward voltage drop, severe reverse recovery voltage and thermal problem.etc. the converter operates probably under hard switching condition, so this makes very poor efficiency of the system. The need of a converter should be like that it has higher switching frequencies. Switching losses associated with turn on, turn off and reverse recovery modules. The efficiency is further reduced, so we need short duty cycle in the case of high input and low output voltage applications. The above mentioned drawbacks of the conventional IBC, we are further intended to develop a new converter which reduces the voltage stress of a buck converter.

In this paper a three level IBC introduced where the voltage stress is half of the input voltage in converters. In a single stage IBC a single capacitor turn off snubber is introduced, then switching loss is reduced but operates in discontinuous conduction mode (DCM). So that the elements suffer from very high current stress. IBC with active clamp circuits is introduced; here all active switches are turned on with ZVS. This creates high conversion ratio and voltage stress across the freewheeling diodes can be reduced. In order to maintain advantages, it requires additional positive elements and active switches, which increases the cost. IBC with zero current transition is introduced to reduce diode reverse recovery losses. The ZCT is implemented by only adding an inductor in to the conventional IBC. But here also the converter suffers from high current stress, because the output current flows in complementary methodology. An IBC with two winding coupled inductors is introduced, has the following advantages, since it operates at continuous conduction mode (CCM), the current stress is lower than that of DCM IBC. The voltage stress is reduced in the semiconductor devices, maintains high power factor [10], switching losses are reduced and gives a high step down conversion ratio[11],[12].

III. Proposed IBC With Input Disturbance

In this paper an IBC is introduced with input voltage disturbance, which is suitable for the applications where the input voltage is high and the operating duty is below 50%.

It is similar to conventional IBC where three active switches are connected in series and a coupling capacitor is employed in the power path. Here the output voltage is regulated by adjusting the duty cycle at a fixed switching frequency. The features of the proposed IBC are similar to those of the IBC. The proposed IBC also operates at CCM, so current stress is low. During steady state the voltage stress across all active switches before turn on / turn off is half of the input voltage. This focuses on capacitive discharging and switching losses can be reduced considerably. The voltage stress of the freewheeling diode is also lower than that of the conventional IBC, reverse recovery and conduction losses on the freewheeling diodes can be improved by employing ordinary schottky diodes that have generally low breakdown voltages. The conversion ratio and output current ripple are lower than those of conventional IBC.

The disturbance circuit is given in the input so as to find the performance of IBC. It is constructed in the simulink model by using two timers, two switches and d.c.voltage source connected as shown in Fig 3a. This will produce an input disturbance of around 6 volts as shown in the Fig 3b, where the variation in the input voltage is noted clearly. Simulation results are given in section IV and Conclusion is present in Section V.

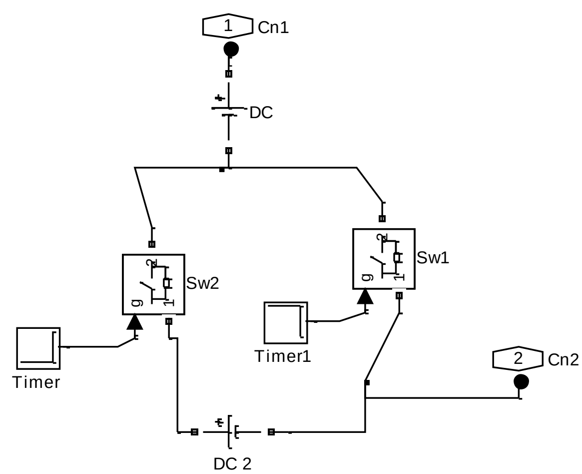

Fig 3a Disturbance Circuit

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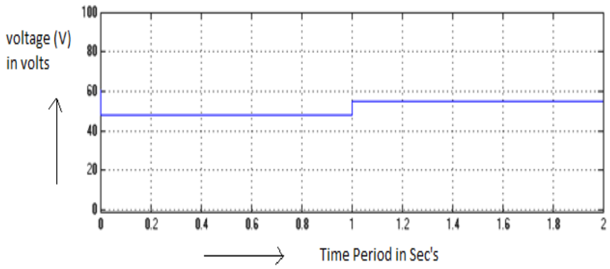

Fig 3b Input Voltage Variation due to disturbance Circuit.

IV. Simulation Results

The technical specifications of the drive systems are as follows :

Input voltage : 48 V AC
After Disturbance : 54 V AC
Buck output voltage : nearly 27 V DC
Pulse width to Buck MOSFET : 0.5 duty cycle (50%)
T_{off} : 50%
Pulse width (33%) to Inverter MOSFET: 120° mode of operation.

Parameters of BLDC Motor are as follows:

The inverter is a MOSFET bridge.
Stator resistance (R_s) : 18.7 ohms
Stator Inductance (L_d, L_s) : 0.02682, 0.02682 Henrys
Flux induced by magnets : 0.1717 Weber's
Back EMF Flat area : 120 degrees
Inertia (J) : 2.26e$^-$005 Kg.m^2
Friction factor (F) : 1.349 e$^-$005 N.m.s
Pole pairs : 2
Stator windings are connected in star to an internal neutral point.

Interleaved Buck converter fed PMBLDC drive system with disturbance circuit is simulated using Matlab/Simulink. The Simulink model of open loop controlled IBC converter fed PMBLDC drive system with input disturbance is shown in Fig 4a. Here 48V AC is rectified by using diode rectifier, and then it is stepped down to 27V DC using an interleaved buck converter. The output of interleaved buck converter is filtered using the elements L & C. The output of rectifier is applied to the three phase inverter. The inverter produces three phase voltage required by the PMBLDC motor.

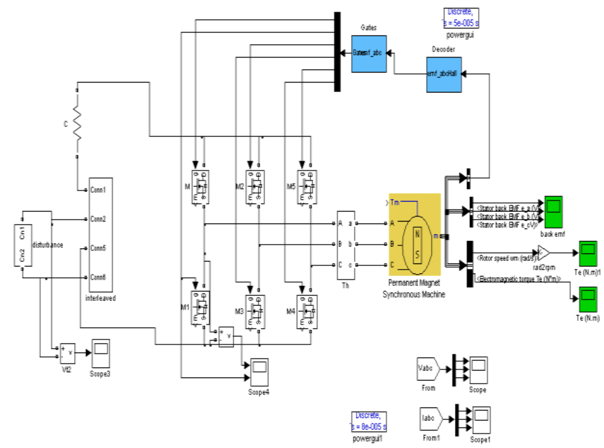

Fig 4a Simulink Diagram of IBC fed PMBLDC drive System with Disturbance Circuit.

The Simulink Diagram of the IBC fed PMBLDC drive system with disturbance circuit is shown in Fig 4a. The input voltage with disturbance is shown in Fig4b. The pulses given to the MOSFETs 1, 3 and 5 of IBC are shown in Fig 4c. The output of the interleaved buck converter is around 27 volts DC, which is shown in Fig 4d.

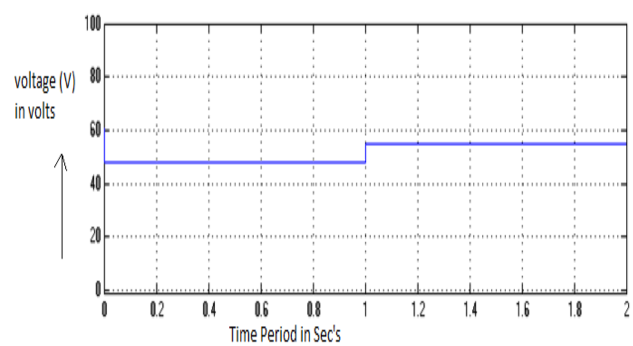

Fig 4b Input Voltage

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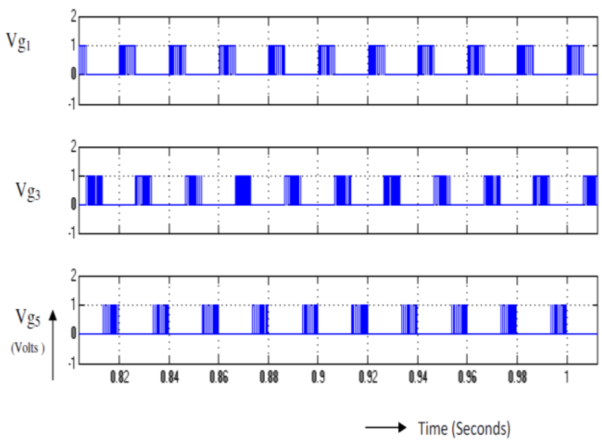

Fig 4c Switching Pulses for M_1, M_3,& M_5 of Inverter.

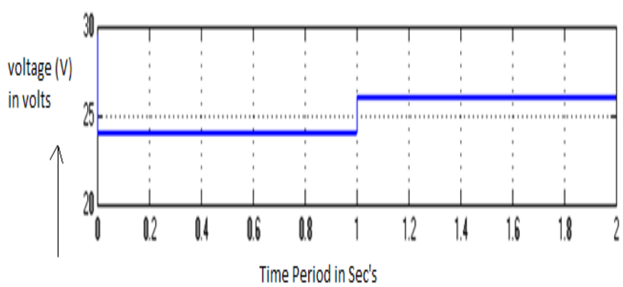

Fig 4d Output Voltage of Interleaved Buck Converter with disturbance circuit

Phase voltages of the three phase inverter are shown in Fig 4e. The voltages are displaced by 120°. Three phase currents drawn by the motor are shown in Fig 4f. The response of speed is shown in Fig 4g. where the speed settles at rated speed.

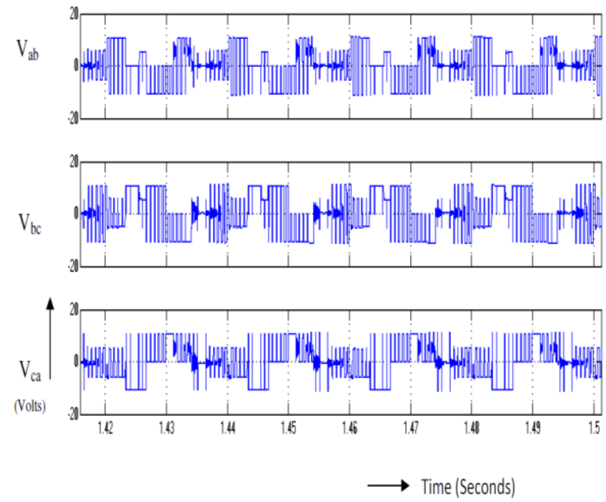

Fig 4e Line to Line voltages of Inverter

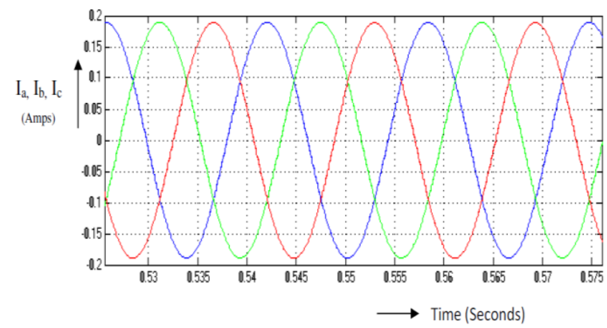

Fig 4f Stator Currents of Motor

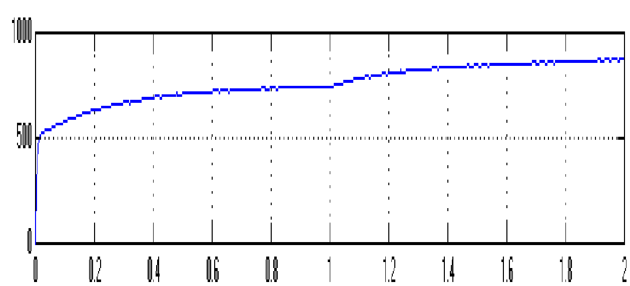

Fig 4g Motor Speed

V. Conclusion

The Interleaved Buck Converter fed PMBLDC drive system with input disturbance circuit is simulated using MATLAB/SIMULINK and the results are presented. A Multi stage IBC with input disturbance is proposed to reduce the input voltage to the required value. Whatever may be the input voltage, the output of the buck converter depends on the duty cycle. L-C filter is proposed at the output of the buck converter to reduce the ripple. This drive system has advantages like reduced voltage stress to switches, improved response and better speed performance is achieved. The scope of this paper is simulation of interleaved buck converter fed PMBLDC drive system with input disturbance circuit. The simulation results are in line with the theoretical results.

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