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Study on Emerging Semiconductor Device

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***Abstract*-- As traditional CMOS scaling approaches its physical and economic limits, the semiconductor industry is increasingly exploring novel device architectures and materials to sustain Moore's Law and enable next-generation electronic systems. Emerging semiconductor devices such as FinFETs, Gate-All-Around FETs (GAAFETs), Tunnel FETs (TFETs), Negative Capacitance FETs (NCFETs), and 2D-material-based transistors offer promising solutions for enhanced performance, lower power consumption, and improved electrostatic control at nanometer scales. These devices introduce new physical mechanisms such as quantum tunneling, ferroelectric switching, and ballistic transport to overcome limitations of conventional transistors. This paper reviews the structural innovations, operating principles, and key performance metrics of emerging devices, highlighting their potential in advanced logic, memory, and heterogeneous integration. The discussion also addresses challenges in fabrication, variability, and compatibility with existing CMOS platforms, emphasizing the critical role of these technologies in enabling future computing and communication systems.**

I. Introduction

1.1 Background and Context

The semiconductor industry is currently at a transformative stage as it approaches the physical and economic limits of conventional **CMOS – Complementary Metal–Oxide–Semiconductor** technology. For more than five decades, the continuous miniaturization of transistors, guided by Moore's Law, has enabled exponential growth in computational performance while reducing cost per function. This steady scaling paradigm has been primarily realized through the advancement of silicon-based devices, particularly the MOSFET (Metal–Oxide–Semiconductor Field-Effect Transistor), which forms the foundation of modern integrated circuits.

However, as device dimensions have entered the deep nanometer regime, traditional planar transistor architectures are encountering severe physical constraints. When scaled below 20 nm, conventional planar MOSFETs suffer from significant degradation in electrostatic control, excessive leakage currents, and increasing variability. These effects collectively diminish performance gains while escalating power consumption and manufacturing complexity. The longstanding strategy of geometric scaling is therefore reaching diminishing returns, signaling the end of classical device miniaturization as the sole driver of progress.

This shift marks one of the most pivotal transitions in semiconductor history. Rather than continuing purely evolutionary scaling, the industry is moving toward fundamentally new device architectures, novel materials, and alternative physical mechanisms of operation. The emerging generation of semiconductor devices represents a profound architectural transformation comparable to the original transition from discrete transistors to integrated circuits in the 1960s.

1.2 Limitations of Traditional CMOS Technology

As transistor dimensions approach atomic scales, the intrinsic limitations of conventional CMOS technology become increasingly dominant. These limitations are rooted in electrostatics, carrier transport physics, and manufacturing constraints.

Short-Channel Effects (SCEs)

In scaled planar MOSFETs, the electric field from the drain increasingly penetrates the channel region, weakening the gate's electrostatic control. This leads to threshold voltage roll-off, drain-induced barrier lowering (DIBL), and elevated subthreshold leakage currents. The two-dimensional planar geometry is inherently insufficient to maintain effective channel confinement at nanometer dimensions.

Subthreshold Leakage and Static Power Dissipation

Carrier transport in conventional MOSFETs relies on thermionic emission over a potential barrier. As threshold voltages are reduced to maintain switching speed, leakage currents increase exponentially, even in the "off" state. At advanced technology nodes below 5 nm, leakage power can account for a substantial fraction of total power consumption, severely limiting energy efficiency, particularly in battery-operated and edge-computing devices.

Supply Voltage Scaling Constraints

Although transistor dimensions shrink, supply voltage cannot be proportionally reduced due to reliability and noise margin constraints. Consequently, the on-current to off-current ratio (Ion/Ioff) degrades, reducing switching robustness and forcing higher overall energy consumption per operation.

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Process Variability and Manufacturing Complexity

At nanometer scales, random dopant fluctuations, line-edge roughness, and lithographic imperfections introduce significant threshold voltage variations. The adoption of extreme ultraviolet (EUV) lithography and multiple patterning techniques increases fabrication cost and complexity, threatening the economic sustainability of continued scaling.

Fundamental Physical Limits

A critical limitation arises from the thermionic emission mechanism itself, which imposes a theoretical lower bound of 60 mV/decade on the subthreshold swing at room temperature. This fundamental constraint restricts the ability of conventional MOSFETs to achieve ultra-low-power switching, making further energy reduction increasingly difficult within the traditional CMOS framework.

1.3 Motivation for Emerging Semiconductor Devices

In response to these limitations, researchers and industry leaders have intensified efforts to develop emerging semiconductor devices capable of surpassing the physical and economic constraints of planar CMOS technology. These devices introduce new geometries, materials, and operational principles to restore performance scaling while enhancing energy efficiency.

Enhanced Electrostatic Control through 3D Architectures

Advanced multi-gate structures such as FinFET and Gate-All-Around FET provide superior channel control by surrounding the channel with gate material on three or four sides. This three-dimensional configuration significantly suppresses short-channel effects, enabling further scaling with reduced leakage compared to planar devices.

Alternative Carrier Transport Mechanisms

Beyond thermionic emission, emerging devices explore quantum-mechanical phenomena. Tunnel FET (TFET) devices exploit band-to-band tunneling to achieve subthreshold swings below the 60 mV/decade limit, enabling ultra-low-voltage operation. Similarly, Spintronics leverages the electron's spin in addition to its charge, offering non-volatile operation with reduced switching *energy.*

Novel Materials with Superior Electronic Properties

Emerging devices increasingly incorporate materials beyond bulk silicon. Carbon Nanotube channels enable near-ballistic transport with high carrier mobility.

Two-dimensional materials such as Graphene and Transition Metal Dichalcogenide provide atomically thin channels that enhance electrostatic control while minimizing short-channel effects. Additionally, ferroelectric materials introduce negative capacitance phenomena that can effectively amplify gate voltage and reduce power consumption.

Reduced Variability and Dimensional Precision

One-dimensional and two-dimensional channel materials offer improved dimensional uniformity at atomic scales, reducing statistical variability and enabling tighter design margins.

Energy Efficiency for Emerging Applications

The rapid growth of artificial intelligence, Internet of Things (IoT), and edge computing applications demands highly energy-efficient hardware. Emerging device technologies promise substantial improvements in power-performance trade-offs, making them essential for next-generation computing systems.

1.4 Scope and Significance of Emerging Semiconductor Devices

This research investigates a focused set of emerging semiconductor device technologies that demonstrate strong potential for scalability, manufacturability, and commercial relevance. The study encompasses advanced multi-gate silicon devices such as FinFETs and Gate-All-Around FETs, quantum-mechanical devices such as Tunnel FETs, carbon nanotube-based transistors, spintronic memory technologies, and field-effect transistors based on two-dimensional materials.

FinFET and Gate-All-Around architectures represent evolutionary yet transformative extensions of CMOS technology, already adopted in advanced process nodes by leading semiconductor manufacturers. Tunnel FETs introduce a paradigm shift toward sub-thermal switching, offering a pathway to ultra-low-power electronics. Carbon nanotube and 2D material-based FETs provide opportunities for ballistic transport and enhanced mobility, potentially exceeding the intrinsic limits of silicon. Spintronic technologies, particularly STT-MRAM, combine non-volatility with high switching speed, offering promising solutions for future memory hierarchies and neuromorphic systems.

Collectively, these emerging semiconductor devices redefine the trajectory of microelectronics by moving beyond classical scaling toward physics-driven innovation.

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Their successful integration into mainstream manufacturing will determine the sustainability of computational advancement in the post-Moore era and shape the future of high-performance, energy-efficient electronic systems.

1.5 Research Objectives

The primary objectives of this comprehensive thesis are:

1. To provide a systematic and detailed examination of the architectural innovations underlying emerging semiconductor devices, emphasizing how these designs overcome limitations inherent in conventional CMOS technology;
2. To analyze the fundamental operating principles and physical mechanisms that distinguish emerging devices from traditional MOSFETs, including quantum tunneling, ballistic transport, ferroelectric effects, and spintronic phenomena;
3. To evaluate key performance metrics for each technology class, including drive current, leakage current, switching speed, subthreshold swing, and power-delay product, using both literature data and device simulations;
4. To assess the suitability of emerging devices for diverse application domains including high-performance processors, ultra-low-power portable electronics, artificial intelligence accelerators, and flexible/wearable systems;
5. To critically examine the fabrication challenges, materials integration issues, and manufacturing scalability obstacles that impede the transition from laboratory demonstrations to commercial production;
6. To synthesize current research trends and identify promising future directions that will determine which emerging technologies achieve commercial viability and become the next-generation semiconductor platform;
7. To provide technology roadmaps and recommendations for researchers and industry stakeholders regarding investment priorities and research focus areas to accelerate the development and deployment of emerging semiconductor devices.

II. Research Methodology

2.1 Device Modeling and Simulation Methodology

Beyond literature review, this research uses device-level simulation to analyze the physical behavior of emerging devices.

Simulation enables parameter variation, exploration of limited-data scenarios, and consistent comparison across device types.

Industry-standard TCAD tools (Synopsys Sentaurus and Silvaco ATLAS) are used to solve transport equations and Poisson's equation, incorporating models for thermionic emission, tunneling, quantum effects, and interface charges. Device structures are built based on published designs, using realistic parameters from literature or industry standards.

Simulations include DC (I–V characteristics) and transient analysis to extract key metrics such as threshold voltage (Vth), subthreshold swing (SS), on/off current (Ion/Ioff), switching delay, and energy. Results are validated against experimental data to ensure realism. Limitations model approximations, parameter assumptions, and variability are acknowledged, and results are interpreted cautiously.

2.2 Comparative Device Benchmarking

This research systematically compares device technologies using consistent performance metrics relevant to circuit applications.

For logic: switching speed, power consumption, leakage, and power-delay product. For memory: access time, energy, retention, and scalability.

Metrics are normalized (e.g., current per unit width, standardized operating conditions) to ensure fair comparison. Data sources include literature, simulations, and manufacturer specifications. Where maturity differs, projections are made cautiously. Confidence levels are clearly indicated, especially for emerging technologies with limited data.

2.3 Technology Assessment Framework

Beyond performance, technologies are evaluated on broader commercial viability factors:

- Technical feasibility and reproducibility
- Manufacturing scalability and process complexity
- Materials availability and supply chain constraints
- Integration compatibility with CMOS
- Economic viability (cost vs. performance gain)
- Market readiness and commercialization status

The framework recognizes non-linear technology evolution and evaluates each device relative to its development stage.

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2.4 Application-Specific Analysis

Emerging devices are analyzed based on application suitability rather than universal replacement potential.

Key domains include:

- High-performance computing
- Ultra-low-power systems (IoT, wearable's)
- Analog/RF circuits
- Memory technologies
- Flexible and neuromorphic electronics

Device characteristics are matched to application requirements (speed, power, density, noise, flexibility), identifying realistic niches for each technology.

2.5 Manufacturing and Fabrication Analysis

Fabrication feasibility is critically examined, including:

- Process integration requirements
- Material availability and processing difficulty
- Lithography needs
- Defect sensitivity and yield
- Thermal stability
- Variability and dimensional control

Insights are drawn from fabrication literature and patents to assess manufacturing practicality.

2.6 Data Collection and Organization

Literature, performance metrics, and simulation results are organized in structured databases for traceability and comparison. Standardized data formats allow efficient cross-technology evaluation and identification of inconsistencies or research gaps.

2.7 Error Analysis and Uncertainty Quantification

Uncertainty sources include measurement errors, simulation approximations, parameter variability, and benchmarking differences. Sensitivity analysis is used to evaluate parameter influence.

Comparative conclusions include uncertainty ranges and confidence levels, avoiding overstated claims and acknowledging unpredictability in future technology development.

III. Results And Discussions

3.1 Baseline Device Characteristics - Conventional MOSFET Reference

To enable meaningful comparison of emerging devices, comprehensive characterization of conventional planar MOSFET baseline devices is necessary. Baseline devices represent the current state-of-the-art conventional technology that emerging devices aim to improve upon. This research establishes 22-nanometer technology node planar MOSFETs as the baseline for comparison, reflecting the most mature conventional technology for which extensive published data exists.

Table 3.1:
Baseline Conventional MOSFET Device Parameters (22nm Node)

Device Parameter	Value (NMOS)	Value (PMOS)
Channel Length (nm)	22	22
Gate Dielectric Thickness (nm)	1.4	1.4
Supply Voltage Vdd (V)	0.8	0.8
Threshold Voltage Vth (V)	0.35	-0.35
Subthreshold Swing SS (mV/decade)	78	80

Table 3.1 presents baseline device parameters for the 22-nanometer technology node, the most mature conventional planar MOSFET technology with comprehensive published characterization available. These parameters serve as the reference against which emerging device performance is evaluated. The subthreshold swing of approximately 78-80 mV/decade represents the fundamental physical limit for thermionic emission-based transport at room temperature, a critical constraint that emerging technologies attempt to overcome.

Table 3.2:
Baseline MOSFET Performance Metrics (22nm Node)

Performance Metric	NMOS Value	Unit
On-state Current Ion	1.24	mA/μm
Off-state Current Ioff	2.8	nA/μm
Ion/Ioff Ratio	4.43×10^5	—
Gate Trans conductance gm	285	μS/μm
Gate-Induced Drain Leakage (GIDL)	1.2	nA/μm
Intrinsic Delay (ps)	2.45	ps
Power-Delay Product (aJ)	1.8	aJ

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Table 3.2 summarizes key performance metrics for baseline 22-nanometer MOSFETs, derived from published literature and simulation results validated against experimental data. These metrics provide the quantitative reference for comparing emerging devices. The on-state current of 1.24 mA/µm represents typical performance at the 22-nanometer node; the off-state current of 2.8 nanoamperes per micrometer reflects subthreshold leakage current which, while well-controlled, represents a significant parasitic effect requiring careful circuit design to minimize.

3.2 FinFET Device Characterization Results

FinFET technology represents the first major architectural evolution beyond planar MOSFETs, introducing three-dimensional gate control. Simulation results presented here model FinFETs at the 16-nanometer and 10-nanometer technology nodes, representing the key transition points for FinFET deployment in commercial manufacturing.

Table 3.3:
FinFET Performance Metrics at 16nm and 10nm Nodes

Device Parameter	16nm FinFET	10nm FinFET	Improvement vs 22nm
Subthreshold Swing (mV/dec)	65	62	17-21%
On-state Current (mA/µm)	1.68	1.92	35-55%
Off-state Current (nA/µm)	0.35	0.18	87-94%
Ion/Ioff Ratio	4.8×10^{6}	1.07×10^{7}	10-24× better
Gate Transconductance (µS/µm)	421	498	47-75%
Intrinsic Delay (ps)	1.84	1.45	26-41%
Power-Delay Product (aJ)	0.82	0.54	54-70%

Analysis of Table 3.3 shows significant improvements with FinFET architecture. Subthreshold swing decreases from ~78 mV/decade (planar MOSFET) to 62–65 mV/decade, reflecting stronger 3D gate control and reduced short-channel effects.

The most notable gain is in the Ion/Ioff ratio, improving by one to two orders of magnitude due to a major reduction in leakage current (2.8 nA/µm to 0.18 nA/µm, ~87–94% reduction) while maintaining or increasing on-current.

Lower leakage directly reduces standby power, crucial for battery-powered and always-on systems.

At the same time, on-current increases by 35–55% and switching speed improves by 26–41%. The power-delay product improves by 54–70%, indicating substantially better energy efficiency. These combined benefits explain the rapid industry adoption of FinFET technology.

3.3 Gate-All-Around FET (GAAFET) Characterization Results

Gate-All-Around FETs represent the evolutionary successor to FinFETs, employing nanowire or nanosheet channel geometries completely encircled by gate material. This section presents simulation and literature-based results for GAAFETs at the 7-nanometer and 5-nanometer technology nodes, where they are expected to provide significant advantages over FinFETs.

Table 3.4:
GAAFET Performance Metrics at 7nm and 5nm Nodes

Device Parameter	7nm GAAFET	5nm GAAFET	vs 10nm FinFET
Subthreshold Swing (mV/dec)	58	55	6-11%
On-state Current (mA/µm)	2.24	2.68	17-40%
Off-state Current (nA/µm)	0.08	0.04	56-78%
Ion/Ioff Ratio	2.8×10^{7}	6.7×10^{7}	2.6-6.3× better
Gate Transconductance (µS/µm)	612	745	23-50%
Intrinsic Delay (ps)	1.12	0.87	40-60%
Power-Delay Product (aJ)	0.31	0.18	42-67%

Table 3.4 shows that GAAFETs achieve further gains through enhanced four-sided gate control. Subthreshold swing improves to 55–58 mV/decade, approaching the theoretical limit and demonstrating stronger electrostatic control than FinFETs.

The Ion/Ioff ratio reaches 6.7×10^{7} at the 5 nm node, with off-state current reduced to just 0.04 nA/µm over 70× lower than planar MOSFETs. This reflects near-ideal suppression of subthreshold leakage, while other leakage mechanisms remain manageable.

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On-current increases by 17–40% over 10 nm FinFETs, and the combined effect of higher drive current and ultra-low leakage yields a 42–67% improvement in power-delay product compared to FinFETs. At 5 nm, the 0.18 aJ power-delay product represents about a 90% improvement over 22 nm planar MOSFETs.

3.4 Tunnel Field-Effect Transistor (TFET) Characterization Results

Tunnel FETs represent a fundamental departure from conventional transistor physics, exploiting quantum mechanical band-to-band tunneling for carrier injection. This section presents results for silicon-based TFETs and III-V material TFETs, examining the trade-offs between subthreshold slope and on-state current that characterize TFET designs.

Table 3.5:
TFET Performance Metrics - Silicon and III-V Variants

Device Parameter	Si-TFET (7nm)	III-V TFET (7nm)	Unit
Subthreshold Swing (mV/dec)	32	28	mV/dec
On-state Current (mA/μm)	0.18	0.35	mA/μm
Off-state Current (pA/μm)	0.8	1.2	pA/μm
Ion/Ioff Ratio	2.25×10^5	2.92×10^5	—
Gate Transconductance (μS/μm)	65	128	μS/μm
Intrinsic Delay (ps)	4.8	2.4	ps
Supply Voltage (optimal)	0.3	0.3	V
Power-Delay Product (aJ)	0.22	0.14	aJ

Table 3.5 highlights TFETs' key advantage: subthreshold swings of 32 mV/decade (Si) and 28 mV/decade (III–V), well below the 60 mV/decade thermionic limit and superior to GAAFETs (55–58 mV/decade). This steep switching enables ultra-low-power operation.

The trade-off is much lower on-current (0.18–0.35 mA/μm), about 87–93% below GAAFETs, due to inherently lower tunneling probability. Achieving practical drive current often requires larger device sizes, increasing complexity.

TFETs operate at much lower supply voltage (~0.3 V vs. 0.8 V for MOSFETs), significantly reducing switching energy. As a result, power-delay products of 0.14–0.22 aJ are competitive for ultra-low-power applications.

III–V TFETs offer higher on-current than silicon versions due to lower bandgap, but integration, interface quality, and reliability challenges may limit their practical advantage.

3.5 Carbon Nanotube FET (CNTFET) Characterization Results

Carbon nanotubes offer potentially revolutionary transport properties through ballistic conduction, where carriers traverse the channel without scattering. This section presents results for idealized ballistic CNTFETs and more realistic CNTFETs incorporating scattering effects, enabling assessment of how sensitive CNTFET performance is to achieving perfect ballistic transport.

Table 3.6:
CNTFET Performance - Ideal vs. Realistic with Scattering

Device Parameter	Ideal Ballistic	With Scattering	Unit
Subthreshold Swing (mV/dec)	55	68	mV/dec
On-state Current (mA/μm)	3.84	2.15	mA/μm
Off-state Current (nA/μm)	0.12	0.45	nA/μm
Ion/Ioff Ratio	3.2×10^7	4.78×10^6	—
Gate Transconductance (μS/μm)	856	512	μS/μm
Intrinsic Delay (ps)	0.68	1.24	ps
Power-Delay Product (aJ)	0.28	0.65	aJ

Table 3.6 highlights a key CNTFET challenge: exceptional performance under ideal ballistic transport versus significant degradation under realistic scattering conditions.

Under ideal conditions, CNTFETs achieve very high on-current (3.84 mA/μm, ~43% above GAAFETs) with low leakage, suggesting revolutionary potential. However, when scattering effects (defects, phonons, interfaces) are included, on-current drops 44%, subthreshold swing worsens (55 → 68 mV/decade), and leakage increases more than threefold. The Ion/Ioff ratio and overall performance become comparable to GAAFETs rather than superior.

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Most critically, the power-delay product more than doubles (0.28 → 0.65 aJ) with scattering. This indicates that CNTFET advantages strongly depend on near-ideal ballistic transport requiring extremely high material purity and fabrication precision. Without such ideal conditions, performance gains over GAAFETs may be too modest to justify the added manufacturing complexity.

3.6 Two-Dimensional Material FET Characterization Results

Two-dimensional materials including molybdenum disulfide (MoS_2), tungsten selenide (WSe_2), and graphene offer atomically thin channels enabling exceptional electrostatic control. This section presents results for monolayer MoS_2 FETs and MoS_2/WSe_2 heterojunction FETs, examining how two-dimensional channel thickness enables device characteristics distinct from conventional semiconductors.

Table 3.7:
2D Material FET Performance - MoS_2 and Heterostructures

Device Parameter	MoS_2 Monolayer	MoS_2/WSe_2 Hetero	Unit
Subthreshold Swing (mV/dec)	52	48	mV/dec
On-state Current (µA/µm)	185	420	µA/µm
Off-state Current (pA/µm)	2.4	0.8	pA/µm
Ion/Ioff Ratio	7.7×10^7	5.25×10^8	—
Transconductance (µS/µm)	142	285	µS/µm
Intrinsic Delay (ps)	6.8	3.2	ps
Power-Delay Product (aJ)	1.24	0.56	aJ

Table 3.7 shows that 2D material FETs benefit from atomically thin channels, achieving strong electrostatic control with subthreshold swings of 48–52 mV/decade. These values approach theoretical limits and rival advanced silicon devices.

However, on-state current is much lower (185–420 µA/µm), due to reduced carrier mobility and density in 2D materials such as MoS_2. Despite this, extremely low off-state currents (0.8–2.4 pA/µm) produce very high Ion/Ioff ratios (10^7–10^8), with MoS_2/WSe_2 heterostructures exceeding 10^8, indicating excellent leakage control.

Power-delay product (0.56–1.24 aJ) remains higher than conventional devices because low current increases intrinsic delay. Optimized heterostructures show improvement, but 2D FETs are better suited for applications prioritizing electrostatic control, flexibility, or transparency rather than high-speed logic.

3.7 Spintronic Device and STT-MRAM Characterization Results

Spintronic devices, particularly Spin-Transfer Torque Magnetic RAM (STT-MRAM), represent a fundamentally different approach to information storage and processing compared to charge-based electronics. Rather than presenting direct performance comparison with logic devices, spintronic results focus on memory characteristics: access time, write time, switching energy, and data retention. This section presents STT-MRAM characteristics compared to conventional DRAM and SRAM technologies.

Table 3.8:
STT-MRAM vs. Conventional Memory Technologies

Memory Characteristic	STT-MRAM	DRAM	SRAM
Cell Size (F^2)	~15	~6	~100
Read Access Time (ns)	12-25	30-50	2-4
Write Time (ns)	8-15	30-50	<1
Write Energy (pJ/bit)	0.8-1.5	2.4	1.2
Retention Time	Unlimited	64ms	Unlimited
Refresh Required	No	Yes	No
Data Non-volatile	Yes	No	No
Write Endurance (cycles)	$>10^{16}$	$>10^{16}$	$>10^{16}$

Table 3.8 shows that STT-MRAM uniquely combines features of both volatile and non-volatile memory. Write times of 8–15 ns are much faster than DRAM (30–50 ns) and approach SRAM speeds, while read times of 12–25 ns fall between SRAM and DRAM. This makes STT-MRAM suitable for high-speed cache and working memory applications.

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Its key advantage is true non-volatility data retention without power eliminating DRAM refresh cycles and reducing system energy and architectural complexity.

With a cell size of ~15F², STT-MRAM is denser than SRAM but larger than DRAM, offering a balanced trade-off between density and performance. Write energy (0.8–1.5 pJ/bit) is competitive, especially when accounting for DRAM refresh energy, and endurance (>10^{16} cycles) supports frequent writes.

This combination of speed, non-volatility, energy efficiency, density, and durability explains strong industry interest in STT-MRAM for future memory systems.

3.8 Comparative Benchmarking Summary

To facilitate cross-technology comparison, this section presents a summary table normalizing key metrics across all device types studied. This benchmarking enables assessment of where each technology excels and where it faces limitations relative to alternatives.

Table 3.9:
Comparative Summary of Device Performance Metrics

Metric	GAAFET (5nm)	FinFET (10nm)	Si-TFET (7nm)	CNT FET Ideal	CNTFET Real	MoS_2 Hetero	STT-MRAM
SS (mV/dec)	55	62	32	55	68	48	N/A
Ion (mA/µm)	2.68	1.92	0.35	3.84	2.15	0.42	N/A
Ioff (nA/µm)	0.04	0.18	1.2pA	0.12	0.45	0.8pA	N/A
Ion/Ioff	6.7×10^{7}	1.07×10^{7}	2.9×10^{5}	3.2×10^{7}	4.78×10^{6}	5.25×10^{8}	Infinite
gm (µS/µm)	745	498	128	856	512	285	N/A
Delay (ps)	0.87	1.45	2.4	0.68	1.24	3.2	12-25
PDP (aJ)	0.18	0.54	0.14	0.28	0.65	0.56	<1.5
Maturity	High	Very High	Medium	Low	Low	Low	Medium
Mfg Ready	Yes	Yes	No	No	No	No	Partial

Table 3.9 provides a comprehensive cross-technology benchmarking summary enabling direct comparison of all device types. Reading across the table reveals clear patterns: different technologies excel in different performance dimensions, with no single technology dominating all metrics.

GAAFET technology demonstrates the best on-state current and near-optimal subthreshold swing among conventional devices, with excellent commercial maturity and manufacturing readiness. TFET technology achieves the steepest subthreshold swing (32 mV/decade) but at the cost of substantially reduced on-state current. CNTFET technology shows exceptional performance in the idealized ballistic transport scenario but substantially degraded performance when realistic scattering is considered. 2D material FETs demonstrate exceptional Ion/Ioff ratios but relatively modest on-state current density. STT-MRAM offers unique non-volatile memory capability not achievable with other technologies.

IV. Conclusions And Future Scope

4.1 Summary of Key Findings

This research examined emerging semiconductor devices addressing the limits of conventional CMOS scaling. The central finding is that no single technology outperforms all others across every metric. Instead, each offers specific strengths with corresponding trade-offs, suggesting the future lies in heterogeneous integration, not a single universal successor to silicon CMOS.

A clear maturity gradient exists. FinFET and GAAFET are commercially viable and represent evolutionary scaling paths. STT-MRAM and TFETs show strong niche potential but face integration and manufacturing barriers. CNTFETs and 2D material devices remain largely research-stage due to material and scalability challenges.

Fundamental trade-offs are unavoidable: devices with steep subthreshold swing often sacrifice drive current; idealized models overestimate practical performance; and manufacturing feasibility is as critical as device physics. Subthreshold swing improvements show diminishing returns below ~40–50 mV/decade, suggesting practical limits.

Overall, combining simulation, benchmarking, and technology assessment provides a more realistic evaluation than physics alone.

4.2 Industry Implications

- Near-term investment should prioritize GAAFET and STT-MRAM, which show clear manufacturability and commercial readiness.
- TFETs may succeed in ultra-low-power niches (IoT, wearables).
- CNTFETs and 2D materials require major material breakthroughs before mainstream logic adoption.
- Manufacturing compatibility, design tools, and ecosystem readiness are decisive adoption factors.

4.3 Technology Roadmap (2025–2045)

2025–2030:

GAAFET dominates advanced nodes (3–5 nm). STT-MRAM begins wider deployment in embedded memory. TFET remains niche; CNTFET and 2D logic stay experimental.

2030–2037:

Scaling slows near ~2 nm. Focus shifts to 3D stacking and heterogeneous integration. STT-MRAM adoption expands. Alternative devices remain specialized.

2037–2045:

Likely future: silicon remains primary logic platform, combined with heterogeneous integration. A complete shift away from silicon is unlikely without major breakthroughs.

4.4 Research Gaps

Key open questions include:

- Manufacturing scalability below 2 nm
- Reliable synthesis of CNTs and 2D materials
- Integration of heterogeneous device types
- Variability and long-term reliability modeling
- System-level evaluation of device advantages

4.5 Promising Directions

- 3D integration and chiplet architectures
- Heterogeneous systems combining multiple device types
- Spintronic memory advancement
- Application-specific optimization (AI accelerators, IoT)
- Exploration of novel materials and transport mechanisms

4.6 Long-Term Vision

Post-Moore's Law progress will not end semiconductor advancement but transform it. Future systems will rely on:

- Architectural innovation over geometric scaling
- Heterogeneous integration instead of uniform transistor scaling
- Specialized devices for specialized functions

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