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Energy-Efficient Transmission Gate FINFET D Flip-Flop for Advanced Memory Cells

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***Abstract*—This work presents the design and performance evaluation of an energy-efficient D flip-flop implemented using transmission-gate (TG) logic in FinFET technology. As device dimensions continue to scale into nanometer regimes, power dissipation and leakage currents have become dominant concerns in memory and sequential circuit design. To address these chal- lenges, the proposed TG-based FinFET D flip-flop is optimized to reduce both static and dynamic power while maintaining reliable switching performance. The design employs FinFET devices with a fin pitch of 48 nm, two fins per finger, a poly pitch of 86 nm, and an 18 nm gate length. With a total transistor count of only 16, the proposed architecture achieves a lower complexity compared to conventional designs that typically require 20–25 transistors. Simulation results demonstrate a static power consumption of 0.3891 nW and a dynamic power of 3.749 nW/MHz, resulting in an average power reduction of approximately 9.36% compared to existing FinFET-based flip-flops. These results confirm that the proposed design is well suited for low-power, high-performance memory cell and sequential logic applications.**

***Index Terms*—Low-power design, Transmission gate (TG), D flip-flop (D-FF), FinFET technology, Leakage power, Dynamic power, Static power, High-performance memory, Energy-efficient circuits, Digital VLSI**

I. INTRODUCTION

The aggressive scaling of CMOS technology into deep- submicron and nanometer dimensions has significantly in- creased power density and leakage currents in modern VLSI circuits [1], [8], [11]. As a result, power consumption has emerged as a critical limitation in the design of high- performance digital systems. Among various circuit com- ponents, sequential elements—particularly D flip-flops (D- FFs)—contribute substantially to total power dissipation due to frequent clock switching activity and leakage paths [2]–[4]. D-FFs serve as the fundamental building blocks of registers, pipelines, and memory architectures, making their energy efficiency crucial for portable electronics, microprocessors, and memory-intensive systems. Reducing power dissipation in flip-flops directly improves overall system performance, battery lifetime, and thermal reliability. Consequently, numer- ous design techniques have been proposed to minimize clock loading, internal node transitions, and leakage currents in flip- flop architectures.

Transmission-gate-based flip-flops have gained attention due to their ability to provide full-swing signal transfer, balanced pull-up and pull-down paths, and reduced clock capacitance [13]–[15]. These properties help lower dynamic power con- sumption and improve timing performance. However, when implemented using conventional planar CMOS technology, TG-based designs remain susceptible to short-channel effects and leakage degradation at scaled technology nodes.

FinFET technology offers improved electrostatic control over the channel, reduced subthreshold leakage, and enhanced drive strength compared to planar CMOS devices [9], [12], [17]. By combining transmission-gate logic with FinFET de- vices, it becomes possible to design D-FFs that achieve both high performance and low power operation. This integration is particularly attractive for advanced memory cell applications such as SRAM, register files, and sequential storage arrays.

This paper focuses on the design and analysis of a transmission-gate-based FinFET D flip-flop optimized for low- power memory applications. The proposed architecture aims to reduce power dissipation while maintaining robust op- eration under process, voltage, and temperature variations. Performance is evaluated through simulation and compared with existing flip-flop designs in terms of power consumption, transistor count, and efficiency.

II. LITERATURE SURVEY

A. Motivation

The increasing demand for energy-efficient digital systems has intensified the need for low-power sequential elements in modern VLSI designs [1], [8], [11]. Since D flip-flops are extensively used in clocked storage elements and memory circuits, even modest improvements in their power efficiency can lead to significant system-level power savings [2]–[4].

Transmission-gate-based flip-flops are attractive for low-power applications because they reduce redundant internal transitions and minimize clock loading [13]–[15]. At the same time, FinFET devices provide lower leakage currents and improved scalability compared to conventional CMOS technologies [9], [12], [17]. Motivated by these advantages, this work explores the combination of TG logic and FinFET technology to develop a compact, power-efficient D-FF suit- able for next-generation memory architectures.

B. Objectives

The main objectives of this research are:

- To design a low-power D-Flip Flop using transmission gate logic optimized for FinFET devices [13], [14].
- To ensure high-speed performance appropriate for memory-intensive applications while minimising dy- namic and static power dissipation [2], [4], [10].
- To compare the suggested design to current TG-based D-FFs and conventional CMOS in terms of resilience, power, propagation delay, and area [3], [15], [16].
- To show how the suggested TG FinFET D-FF can be used in low-power memory architectures such sequential logic storage and SRAM [5], [22], [24].

C. Review of Previous Works

Important information about low-power flip-flop and mem- ory designs can be found in earlier research:

- Yuan and Svensson [1]investigated the core high-speed CMOS circuit design methodologies.
- Zhao *et al.* [2] suggested a low-power flip-flop that greatly decreased dynamic power by reducing the clock burden.
- Lee *et al.* [3] and Wang and Wang [4] demonstrated low- power flip-flops designed for high-performance uses.
- Sahoo *et al.* [13] and Shah *et al.* [14] examined TG- based D-FFs and showed the advantages of energy and area efficiency.
- Lee *et al.* [15] and Alioto and Palumbo [16] researched TG flip-flops under process, voltage, and temperature (PVT) alterations, stressing their capacity for resilience.
- Sun *et al.* [9] and Duarte *et al.* [12] concentrated on FinFET-based circuit optimisation, demonstrating en- hanced performance and decreased leakage.
- Taghipour and Asli [17] highlighted the reliability ben- efits of FinFET by comparing the ageing of CMOS and FinFET flip-flops.
- Verma and Chandrakasan [5], Arunkumar *et al.* [22], and Dhanasekar *et al.* [20], [24], [25] shown the value of energy-efficient D-FFs in system-level applications and low-power memory systems.

D. Research Gap

Although transmission-gate-based flip-flops effectively re- duce dynamic power in CMOS implementations, relatively few studies have explored their optimization using FinFET technology for memory-oriented applications. Furthermore, many existing works evaluate power or delay independently, without providing a unified analysis of power, area, and robustness under scaled technology conditions. This research addresses these limitations by proposing a compact TG-based FinFET D flip-flop and evaluating its performance for low- power memory systems.

E. Summary

Previous studies have explored a wide range of low-power flip-flop architectures aimed at minimizing clock power, leak- age current, and propagation delay. Early work by Yuan and Svensson [1] established fundamental principles for high- speed CMOS design. Subsequent research focused on reducing clock-related power dissipation in sequential circuits [2]–[4]. Transmission-gate (TG) based designs have been demonstrated to improve energy efficiency by lowering transistor count and reducing internal node switching [13], [14].

More recent studies have examined the effects of process, voltage, and temperature (PVT) variations on TG-based flip- flops, emphasizing their robustness under diverse operating conditions [15], [16]. In parallel, FinFET-based circuit im- plementations have shown superior leakage control and en- hanced performance scalability compared to conventional pla- nar CMOS designs [9], [12], [17]. Despite these advancements, there remains limited research addressing the integration of TG logic with FinFET technology specifically for low-power memory cell applications, which motivates the development of the proposed design.

F. Analysis of D Flip-Flop

At the clock signal's active edge, it samples the input data (D) and holds onto the result (Q) until the subsequent clock event. This in memory cells, registers, and control circuits, behaviour guarantees dependable data storage and synchronisation. Clock-to-Q delay, hold time, and setup time are some of the elements that define a D Flip-Flop's per- formance.

These parameters specify the system's maximum operating frequency and timing restrictions. Process, voltage, and temperature fluctuations make it more difficult to maintain timing dependability as technology grows. D Flip-Flops utilise both static power from leakage currents and dynamic power from clock switching activity. The clock network drives a lot of flip-flops, therefore inefficient designs can significantly raise the total dissipation of power. Consequently, lowPower D-FF designs prioritise minimised clock load, Leakage reduction and internal switching. For low-power and high-density memory cell architectures, advanced DFlip-Flop implementations util- ising transmissiongate logic and FinFET technology provide increased performance, decreased leakage power, and higher energy efficiency.

G. Proposed D-Flip Flop

Flip-flops are essential components of digital systems, mainly utilised for clock signal synchronisation and data storage.

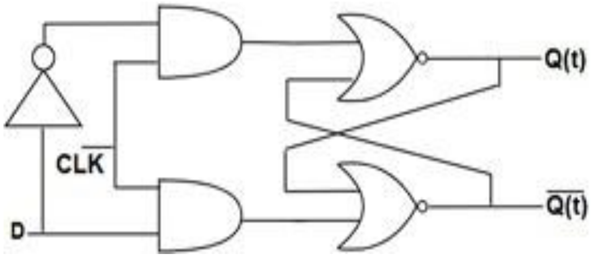

Fig. 1. Traditional D-Filp Flop Circuit Diagram

Adoption of transmission gates with effective Switching behaviours reduce power consumption, propagation time, and silicon area while dramatically improving circuit per- formance. The transmission gatelogic-based low-power Dflip flop presented by Sahoo et al. delivers significant power dissipation savings by avoiding redundant transitions in the clock network [13]. Therefore, these transmission-gate-based designs are ideal for battery-powered and portable applications where energy efficiency is a critical need. In order to achieve low-power operation, the suggested design, shown in Fig. 2, is a transmission gate (TG)-based FinFETD flip-flop constructed utilising high threshold voltage (HVT) cells.HVT cells con- siderably lower leakage current and total power consumption when compared to standard threshold voltage (SVT) and low threshold voltage (LVT) cells. Because of this, the suggested flip-flop is ideal for low-power pipeline stages in contemporary CPU architectures.

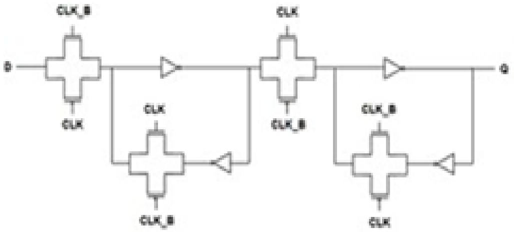

Fig. 2. Transmission Gate D-Filp Flop

Additionally, efficient area minimisation is made possible by the small structure of transmissiongate-based flip-flops, which is particularly advantageous in tightly packed VLSI circuits. A transmission gate-based flip-flop design with roughly 30% less transistors without sacrificing performance was reported by Shah et al. [14]. This makes it perfect for applications with limited space, such register files and cache memory. In addi- tion to saving chip space, a lower transistor count also lowers leaking power, enhancing scaled technological nodes' energy efficiency. Lee et al. suggested a gearbox gate Dflip-flop architecture with adaptive body biassing to increase tolerance against process, voltage, and temperature (PVT) fluctuations in order to further improve reliability. The suggested method is appropriate for mission-critical applications like automotive and aerospace systems because it showed steady and reliable functioning under a variety of environmental circumstances [15]. Transmission gates offer complete voltage swing oper- ation and enhanced signal integrity when compared to con-ventional pass-transistor logic techniques. Additionally, Alioto and Palumbo demonstrated that by enabling data transfer with minimum voltage deterioration, transmissiongate-based flip- flops preserve better noise margins [16].

A. Analysis of Memory Cell

See Fig. 3. The basic building block of a digital memory system that holds a single bit of data is called a memory cell. It is essential in assessing the total power and performance usage and memory architecture dependability. Data stability, quick read/write operations, and minimal power consumption are essential components of a memory cell. Parameters including access time, retention time, noise margin, and leakage current affect memory cell performance.Leakage power has taken front stage due to rapid technological scaling, particularly in high-density memory arrays.Low-power design strategies are therefore crucial for increasing energy efficiency while preserving data integrity.

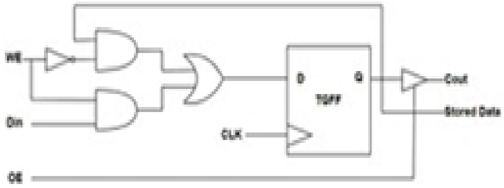

Fig. 3. Memory Cell Diagram

Advanced device technologies such as FinFETs offer improved electrostatic control and reduced leakage compared to conventional CMOS devices. When combined with energy-efficient storage elements like optimized D flip-flops, FinFET-based memory cells achieve enhanced performance, reduced power consumption, and improved scal- ability for modern memory applications.

B. Algorithm for Proposed D-Flip Flop

Algorithm: Design of Energy-Efficient TG FinFET D-Flip Flop

1) Begin the design process.
2) Perform a detailed literature survey on low-power D flip- flop architectures.
3) Analyze the limitations of conventional CMOS and pass- transistor flip-flops.
4) Select transmission gate logic with FinFET technology for low-power operation.
5) Design the TG-based FinFET D flip-flop circuit using HVT cells to reduce leakage power.
6) Implement the circuit schematic using Tanner EDA version 16.
7) Perform pre-layout simulations to verify functional cor- rectness.
8) Measure performance parameters such as power con- sumption and propagation delay.
9) Design the physical layout of the proposed flip-flop.
10) Perform post-layout verification including DRC and LVS checks.
11) Analyze layout-aware performance metrics such as power, delay, and area.
12) Optimize the design to achieve minimum power dissi- pation and reduced silicon area.
13) Examine the final design and monitor the simulation's outcomes.
14) Wrap up the design process.

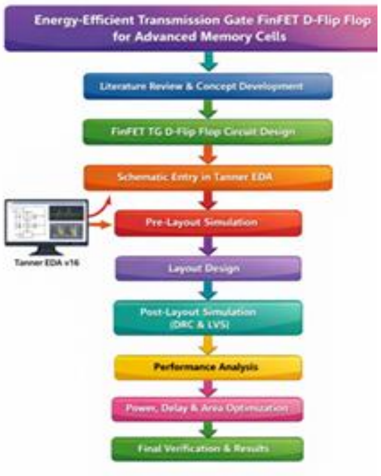

Fig. 4. Flow Chart

III. RESULTS AND DISSCUSSIONS

Effective data transport and storage are made possible by the use of a Dflip-flop, which uses the clock and its complemen- tary signal to regulate transmission gates. NMOS and PMOS transistors, which combined enable full swing signal propaga- tion and reduce the threshold voltage loss frequently observed in passive transistor designs, are used in the construction of the transmission gates. Below Fig 5 shown as , High-threshold- voltage (HVT) NMOS and PMOS transistors are used in the design to achieve low-power operation.By minimising static power consumption, the usage of HVT devices considerably lowers leakage current when the flip-flop is in the idle or data- holding state. This feature is particularly advantageous in deep submicron VLSI technologies, where leakage power takes centre stage.

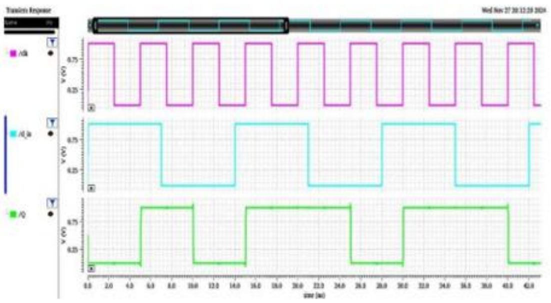

Fig. 5. TGFF Output Waveform

TABLE I
FOR TG FFINFET TECHNOLOGY PARAMETERS

SNo	Fin Pitch	No.of Fins/Finger	Poly Pitch	Drawn Gate Length
1	48nm	2	poly86	18nm

According to Table I , The transmission-gate-based paraphase D flip-flop minimises needless internal switching activity when compared to conventional flip-flop topologies. This decrease reduces the dynamic power dissipation during switching transitions. Furthermore, the streamlined transistor arrangement guarantees robust edge-triggered operation and improves dependability.

TABLE II
PERFORMANCE PARAMETERS OF FINFET FF'S

FINFET FF'S	HLFF[17]	SDFF[18]	USDFF[19]	Proposed TGFF
Transistor count	20	23	25	16
Static Power	1.97	3.35	4.53	0.38
Dynamic Power	9.18	3.32	3.75	3.74
Average Power	9.05	3.74	3.98	3.63

Table II shows, Overall the HVT NMOS and PMOS transistors used in the paraphase trans- mission gate flip-flop demonstrate increased energy efficiency and decreased power consumption, as well as strong perfor- mance. These benefits make it suitable for low-power applica- tions in contemporary VLSI systems, such as memory cells, registers, and sequential logic circuits.

A. D Flip-Flop Operation

The output waveform of a D flip-flop illustrates how the circuit reacts when the clock signal (CLK) and data input (D) are applied.One of the essential components of sequential logic circuits, the D flip-flop samples the input data at a certain clock transition, usually at the rising edge.The output Q records and takes on the value of the input D to teach an active clockedge. Regardless of changes at the input, the output stays constant during the clock period after the data is latched until the next clock edge.This action guarantees that the output and the clock signal are completely synchronised, so avoiding unwanted data transitions and supplying steady, dependable data for the circuit's later stages. Thus, in sequential systems, the paraphase D flip-flop provides synchronised and error-free operation. [22], [23].

B. Contrasting Conventional Designs

When compared to traditional designs like the US DFF, the suggested transmission-gate-based FinFET D flop with an improvement of up to 9.36The usage of transmission- gates, which naturally have reduced pasitic capacitance, is the main cause of this decrease.

As a result, there is less needless switching, which improves signal flow and lowers dynamic power dissipation [24], [25]. Furthermore, because the transmission-gate structure requires fewer transistors than conventional latch-based implementations, the suggested ar- chitecture has a smaller area overhead. The suggested D flip- flop is highly suited for low-power and area-efficient VLSI applications because it retains strong performance without sacrificing speed or functionality despite its small layout.

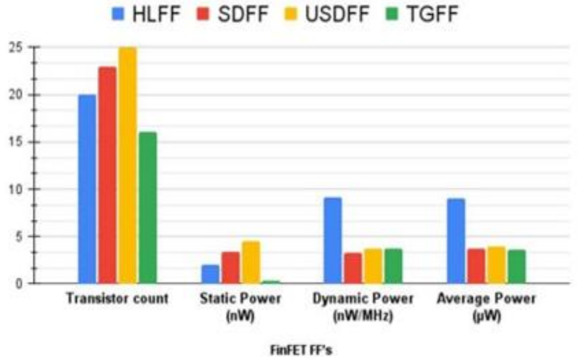

Fig. 6. Examination of different FINFET methods

IV. CONCLUSION

When compared to traditional designs, the suggested Trans- mission Gate (TG) based FinFET D Flip Flop shows a notable increase in power efficiency. The suggested TGFF design achieves the lowest transistor count (16), as indicated in Table II, which helps to lower complexity and area. Furthermore, the dynamic power is minimised to 3.749 nW/MHz and the static power is drastically decreased to 0.3891 nW. This results in an average power consumption of 3.631 µW, which is roughly 9.36% less than traditional FinFETD-Flip Flops.These findings verify that the TG-based design maintains dependable performance at high frequencies while offering low power op- eration. The design provides an effective solution for energy- constrained applications, especially in memory cell designs, by fusing the benefits of TG logic with FinFET technology.

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