

# Selective Harmonic Elimination and Space Vector PWM for a High-Level Cascaded Multilevel Inverter

S. Naveena<sup>1</sup>, K. Asokan<sup>2</sup>

<sup>1</sup>Assistant Professor, Department of Electrical and Electronics Engineering, Jayalakshmi Institute of Technology, Thoppur, Dharmapuri, Tamil Nadu, India, 636352.

<sup>2</sup>Associate Professor, Department of Electrical and Electronics Engineering, Government College of Engineering, Bargur, Tamil Nadu, India, 635104.

**Abstract**--Multilevel inverters have become increasingly significant in high-power and high-voltage applications due to their ability to synthesize high-quality output voltages with low harmonic distortion. Among the various multilevel inverter topologies, the cascaded H-Bridge configuration is widely used for its modular structure and scalability. This paper presents a hybrid modulation technique for a 27-level cascaded H-Bridge multilevel inverter, aimed at minimizing harmonic distortion while maintaining high efficiency and performance. The proposed method integrates Selective Harmonic Elimination Pulse Width Modulation (SHE-PWM) and Space Vector Pulse Width Modulation (SVPWM) techniques. SHE-PWM is applied to eliminate specific lower-order harmonics, namely the 3rd and 5th, which are typically dominant and detrimental to power quality. By precisely controlling the switching angles, SHE-PWM significantly reduces total harmonic distortion (THD). In parallel, SVPWM is utilized to increase the effective number of voltage levels in the output waveform, which enhances the waveform quality and further reduces harmonics. The combination of these two techniques enables optimized harmonic suppression, better voltage control, and reduced electromagnetic interference. MATLAB/Simulink is used to model and simulate the proposed inverter system. The simulation results confirm the effectiveness of the hybrid modulation scheme, demonstrating significant improvement in waveform quality and a considerable reduction in THD compared to conventional PWM methods. The proposed strategy is suitable for medium to high-voltage industrial applications where power quality and efficiency are critical. Future work will focus on experimental validation and the implementation of real-time control algorithms for practical deployment.

**Keywords:** Multilevel Inverter, Cascaded H-Bridge, Selective Harmonic Elimination, Space Vector PWM, Total Harmonic Distortion

## I. INTRODUCTION

Multilevel inverters (MLIs) have gained significant attention in recent years, particularly for medium to high-voltage applications, owing to their capability to generate output voltages with superior waveform quality, reduced harmonic distortion, and enhanced efficiency.

By synthesizing stepped output voltages through the combination of multiple voltage sources, MLIs reduce the voltage stress on power devices and minimize the need for bulky output filters. Among the various topologies, the Cascaded H-Bridge (CHB) multilevel inverter has emerged as a preferred configuration due to its modular structure, scalability, fault-tolerant capabilities, and the ability to operate without the need for complex voltage balancing circuits [1-3].

The performance of multilevel inverters is heavily dependent on the adopted modulation technique, which directly affects total harmonic distortion (THD), switching losses, and overall system efficiency. Conventional sinusoidal pulse width modulation (SPWM) techniques, although simple to implement, often result in higher THD and less efficient voltage utilization, especially as the number of levels increases. To overcome these limitations, advanced techniques such as Selective Harmonic Elimination PWM (SHE-PWM) and Space Vector PWM (SVPWM) have been explored extensively [4-6].

SHE-PWM is a harmonic mitigation strategy that eliminates specific lower-order harmonics, such as the 3rd, 5th, or 7th, by solving transcendental equations for optimal switching angles. This technique offers excellent harmonic control while maintaining relatively low switching frequency, making it ideal for high-power applications. Numerous studies have demonstrated the effectiveness of SHE-PWM in reducing low-order harmonics in CHB inverters. For instance, Pourdashnia et al. [7] and Sadoughi et al. [8] have shown that optimization algorithms like Particle Swarm Optimization (PSO) and Artificial Neural Networks (ANN) can be effectively employed to solve switching angle equations in real time, thereby extending the applicability of SHE-PWM to a broader range of operating conditions. However, SHE-PWM alone can be limited at low modulation indices, where it becomes increasingly difficult to find feasible solutions for angle equations, leading to higher residual harmonics.

On the other hand, SVPWM offers superior DC-link voltage utilization and reduced THD compared to traditional PWM methods. It works by representing the desired output voltage as a combination of adjacent space vectors and is particularly effective in three-phase inverter systems. Recent works, such as those by Shruthi et al. [9] and Mao et al. [10], have shown that SVPWM techniques can be extended to multilevel topologies, including CHB inverters, to further enhance output quality. However, SVPWM alone may not effectively eliminate specific low-order harmonics unless combined with additional control strategies.

To address the limitations of individual techniques, hybrid modulation schemes have been proposed that combine the strengths of both SHE-PWM and SVPWM. These strategies aim to reduce specific harmonics using SHE while employing SVPWM to increase the number of effective switching states and improve waveform smoothness. For example, Wang et al. [11] presented a hybrid modulation technique for photovoltaic-fed CHB inverters that significantly enhanced output waveform quality. Despite these advancements, most existing research focuses on low- or mid-level inverter configurations (e.g., 5-level or 7-level), with limited literature available on hybrid modulation applied to very high-level inverters (e.g., 27-level CHB systems). Moreover, the implementation complexity and computational burden of such hybrid schemes for high-level inverters remain underexplored [12-15].

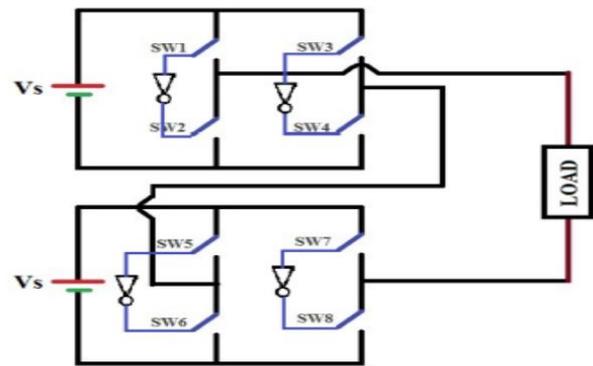
This paper proposes a novel hybrid modulation strategy that integrates SHE-PWM and SVPWM for a 27-level CHB inverter. The SHE-PWM technique is employed to eliminate dominant low-order harmonics, specifically the 3rd and 5th, through precise switching angle control. Simultaneously, SVPWM is applied to enhance the effective number of voltage levels in the output waveform, thereby further reducing THD and improving spectral quality. The system is modeled and simulated in MATLAB/Simulink, and the results confirm that the proposed hybrid approach significantly outperforms traditional modulation techniques in terms of harmonic reduction and waveform quality. The method is particularly suitable for high-voltage industrial applications where power quality, reliability, and efficiency are critical.

## II. PROPOSED MODEL DESCRIPTION

### A. Existing System

The existing system uses a five-level cascaded H-Bridge inverter with a harmonic elimination technique based on Chebyshev polynomials.

This method calculates optimal switching angles to eliminate low-order harmonics, such as the 3rd and 5th, by solving simplified mathematical equations [16]. The approach reduces total harmonic distortion (THD) while maintaining a good quality output waveform. However, it is best suited for low-level inverters and becomes complex to scale for higher-level configurations.

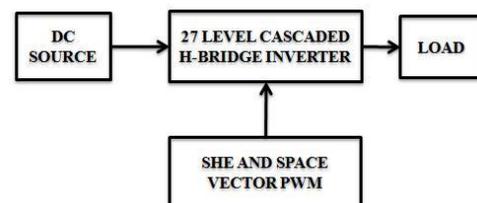


**Fig 1 Circuit diagram for existing system**

Fig. 1 illustrates the circuit diagram of a five-level cascaded H-Bridge multilevel inverter. The system consists of two H-Bridge inverter modules connected in series per phase, each powered by an isolated DC voltage source. The switching devices (typically IGBTs or MOSFETs) in each H-Bridge are controlled using gate pulses generated from pre-calculated switching angles. These angles are determined using Chebyshev polynomials to eliminate selected harmonics, improving the quality of the output voltage. The output is then applied to the load, producing a stepped waveform with reduced harmonic distortion.

### B. Proposed Asymmetrical 27 Level Multi-inverter

Fig 2 represents the Asymmetrical Cascaded H-Bridge Inverter topology. In the proposed work 27 level cascaded h bridge inverter with hybrid PWM. This hybrid PWM consist of selective harmonic PWM and Space vector PWM. In this system we are used 8 number of switches for this level of multilevel inverter.



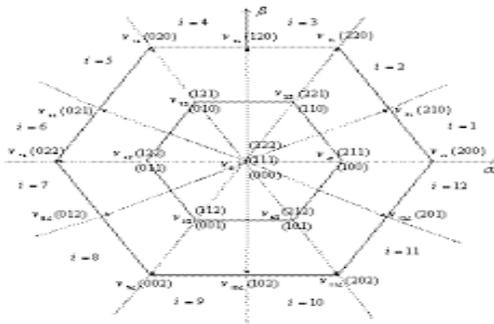
**Fig 2 Block diagram for 27 level multi inverter**

This 27 level of output is obtained with reduced switches. In multilevel inverter cascaded inverter configuration attracts more research attention than flying-capacitor and diode clamped due to their circuit simplicity and modularity. The number of levels in output voltage can be increased either by increasing the number of H-Bridges or by providing different sources (Asymmetrical configuration) with particular voltage ratio among bridges or combination of both. Providing different voltage sources with suitable number of bridges with particular voltage ratio provide required number of output voltage level with circuit modularity and easy.

### III. SELECTIVE HARMONIC ELIMINATION AND SPACE VECTOR PWM

#### a. Multilevel Space Vector PWM

The space vector modulation (SVM) algorithm is basically also a PWM strategy with the difference that the switching times are computed based on the three-phase space vector representation of the reference and the inverter switching states rather than the per-phase in time representation of the reference and the output levels as in previous analysed methods [17-18].



**Fig 3 Vector diagram for three level Space Vector Modulation**

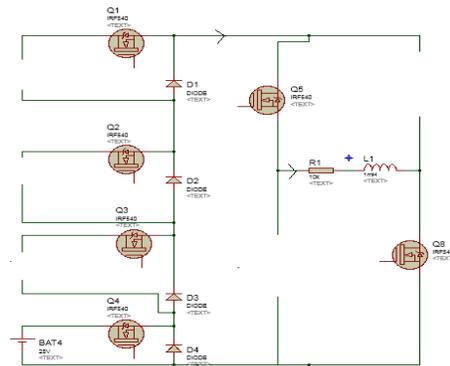
#### b. Multilevel Selective Harmonics Elimination

The Selective Harmonic Elimination PWM (SHE PWM) technique is currently applied in conventional twenty seven level inverter circuits [19-20]. It needed to be compared to the optimized harmonic stepped-waveform technique in several aspects. Mainly, the harmonic components and the harmonic characteristics will be focused. SHE techniques can be applied to cascade multilevel inverters using two approaches. The first one is to consider one commutation angle per inverter; thus, the number of harmonics that can be eliminated is  $N_{inv} - 1$ .

### IV. SWITCHING MODE OF OPERATION FOR 27 LEVEL INVERTER

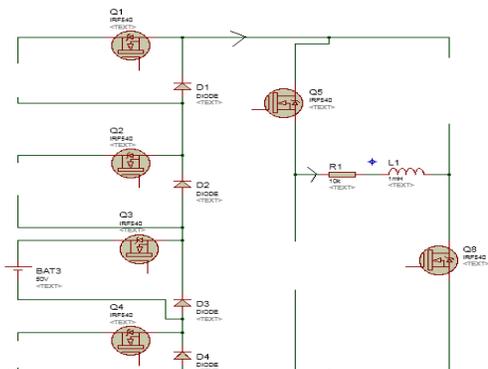
The switching modes of operation for 27 level multi inverter are shown below. It contains 8 MOSFET switches. Here every positive levels are shown separately.

#### MODE 1:



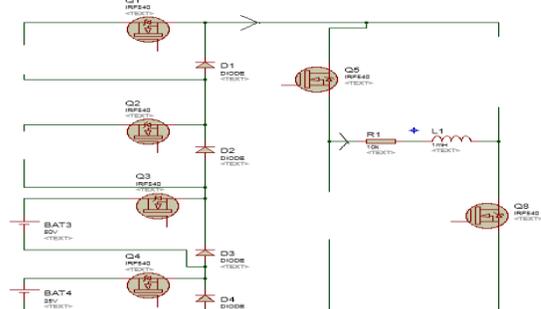
**Fig 4 Mode 1 for Multilevel Inverter**

#### MODE 2:



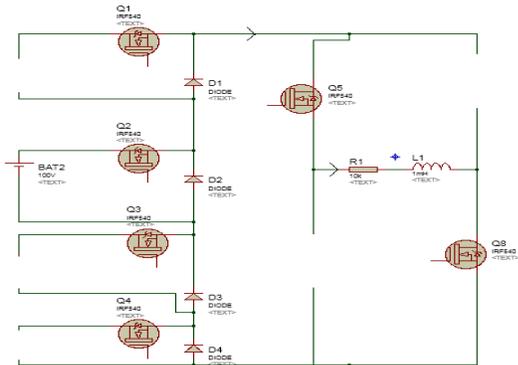
**Fig 5 Mode 2 for multilevel inverter**

#### MODE 3:



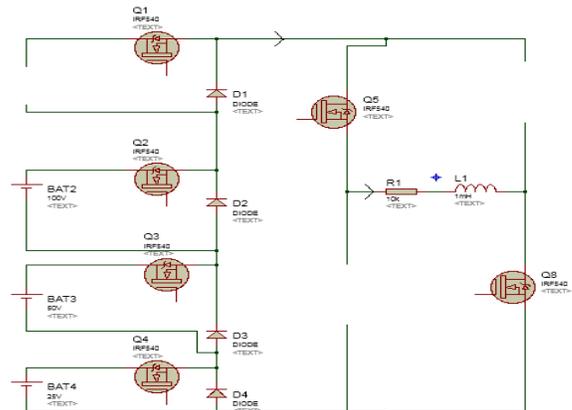
**Fig 6 Mode 3 for multilevel inverter**

**MODE 4:**



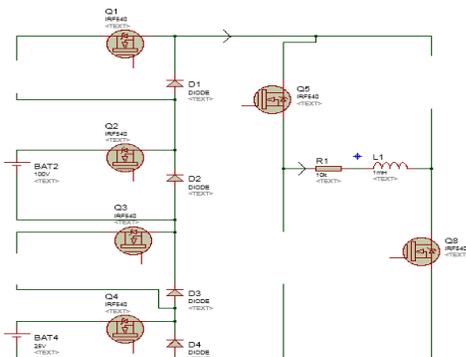
**Fig 7 Mode 4 for multilevel inverter**

**MODE 7:**



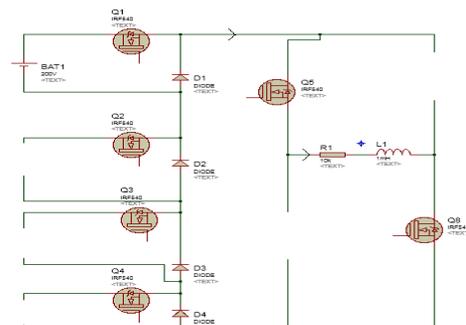
**Fig 10 Mode 7 for multilevel inverter**

**MODE 5:**



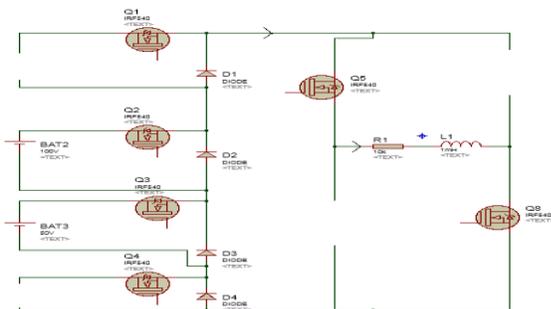
**Fig 8 Mode 5 for multilevel inverter**

**MODE 8:**



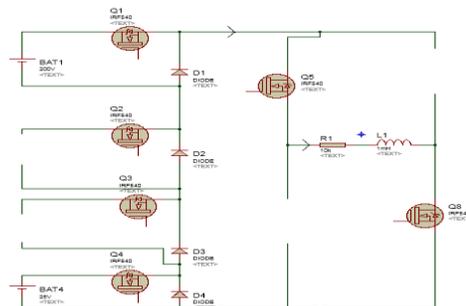
**Fig 11 Mode 8 for multilevel inverter**

**MODE 6:**



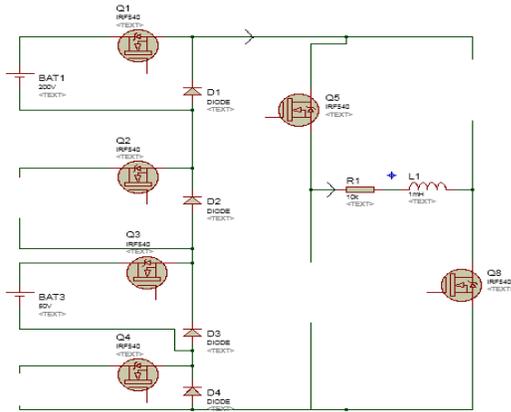
**Fig 9 Mode 6 for multilevel inverter**

**MODE 9:**



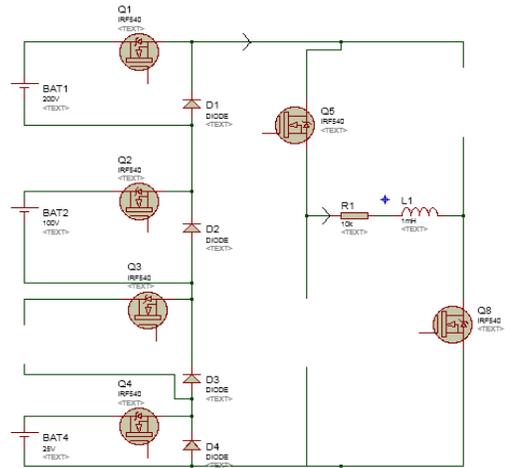
**Fig 12 Mode 9 for multilevel inverter**

**MODE 10:**



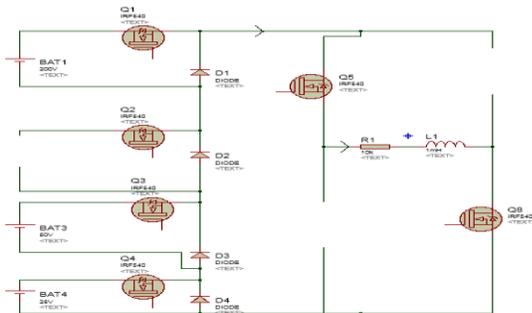
**Fig 13 Mode 10 for multilevel inverter**

**MODE 13:**



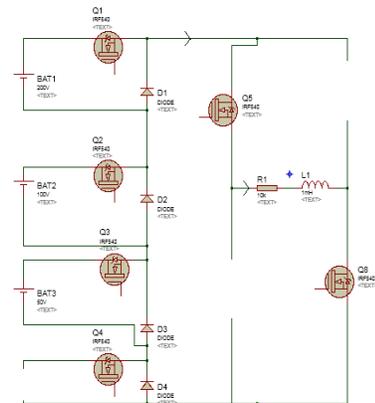
**Fig 16 Mode 13 for multilevel inverter**

**MODE 11:**



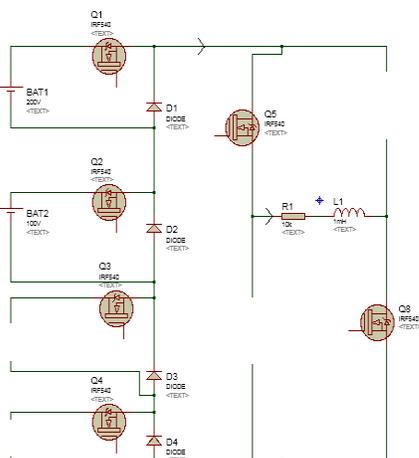
**Fig 14 Mode 11 for multilevel inverter**

**MODE 14:**



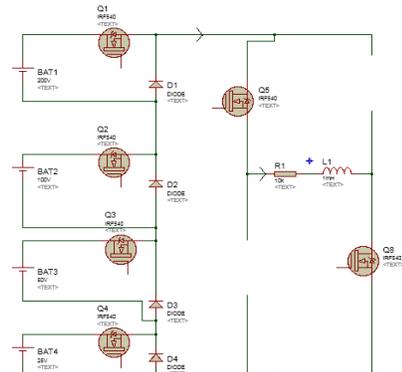
**Fig 17 Mode 14 for multilevel inverter**

**MODE 12:**



**Fig 15 Mode 12 for multilevel inverter**

**MODE 15:**



**Fig 18 Mode 15 for multilevel**

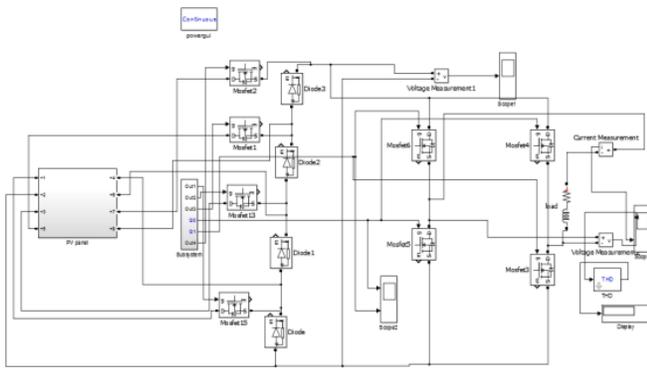
These are the switching modes operation for 27 level multi inverter. Here every modes are shown separately and input voltages are t started from 25V to 375V respectively.

### V. SIMULATION RESULTS AND DISCUSSION

To evaluate the effectiveness of the proposed hybrid modulation strategy combining Selective Harmonic Elimination (SHE-PWM) and Space Vector PWM (SVPWM), a 27-level cascaded H-Bridge multilevel inverter was modeled and simulated in MATLAB/Simulink. The simulation was performed under balanced load conditions using a resistive-inductive (R-L) load, and the switching pattern was derived from pre-calculated SHE angles and SVPWM vector sequencing. The simulation results are presented and discussed in the following subsections.

#### A. Simulation Diagram

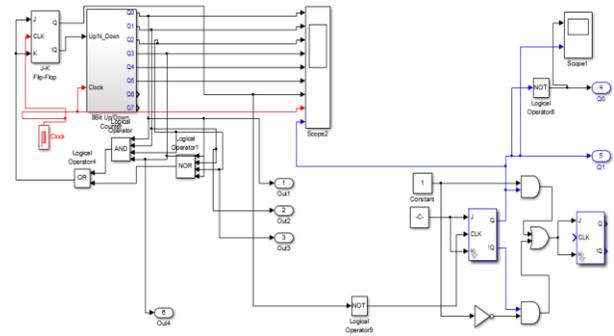
The complete simulation model is shown in fig 19, which illustrates the modular structure of the 27-level cascaded H-Bridge inverter. The model consists of nine H-bridge units per phase, supplied by separate DC sources to generate the desired voltage steps. The control subsystem implements the hybrid modulation logic that generates the required switching signals for each power device.



**Fig 19 Simulation of cascaded multilevel inverter**

#### B. Pulse Generation

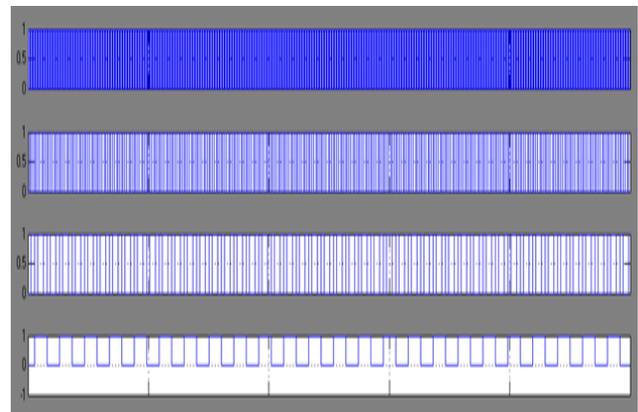
Fig. 20 displays the pulse generation block output. The SHE-PWM module computes optimal switching angles to eliminate the 3rd and 5th harmonics. These switching angles are then mapped onto the timing sequence of the pulse generator. The SVPWM logic further refines the timing by calculating the appropriate space vectors within the SHE-defined windows to achieve a smoother voltage transition and increase the effective number of output levels.



**Fig 20 Pulse generation of proposed model**

#### C. Pulses for Level Creator

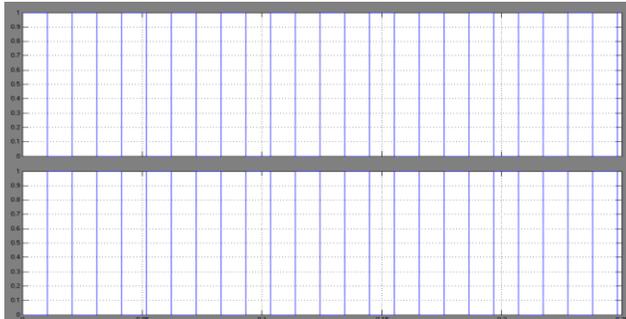
As shown in fig. 21 the level creator pulses are responsible for generating intermediate voltage steps from the combination of multiple H-bridge outputs. Each bridge operates with precise timing to ensure proper stacking of voltages. The result is a staircase-like waveform with 27 distinct levels per half-cycle. These levels help to approximate a sinusoidal output with high fidelity.



**Fig 21 Pulses for level creator**

#### D. Pulses for H-Bridge Inverter

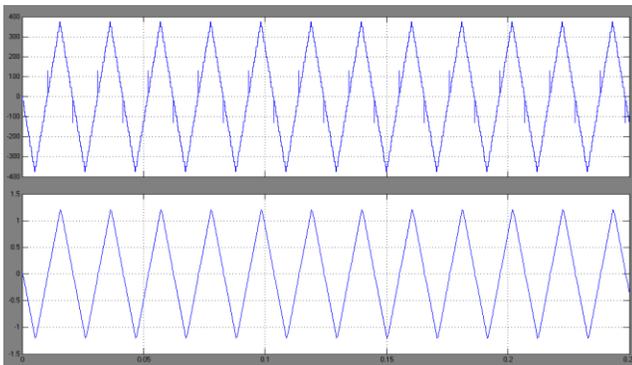
Fig. 22 illustrates the switching signals applied to the H-Bridge inverters. The hybrid modulation ensures that each H-bridge switches at the exact time calculated through the SHE-PWM algorithm, while within those windows, SVPWM logic improves switching efficiency and reduces voltage stress on individual switches. The combination significantly reduces switching losses while maintaining harmonic performance.



**Fig 22 Pulses to H bridge inverter**

### E. Output Voltage and Current Waveforms

Fig. 23 shows the output voltage and current waveforms of the 27-level inverter under load. The voltage waveform exhibits a nearly sinusoidal shape with 27 discrete levels per half cycle, confirming the successful synthesis of the stepped waveform. The output current closely follows the voltage waveform, indicating proper power delivery and load compatibility.



**Fig 23 Output voltage and current waveform**

The Total Harmonic Distortion (THD) of the output voltage was measured to be approximately **1.92%**, significantly lower than what is typically achieved with conventional SPWM or SVPWM methods alone. This demonstrates the effectiveness of combining SHE-PWM for eliminating targeted low-order harmonics with SVPWM for improving voltage waveform smoothness and utilization. Compared to a pure SHE-PWM approach, the hybrid technique results in reduced harmonic content, improved waveform symmetry, and enhanced control over voltage levels.

### VI. CONCLUSION

This paper presented a hybrid modulation strategy combining Selective Harmonic Elimination (SHE-PWM) and Space Vector Pulse Width Modulation (SVPWM) for a 27-level cascaded H-Bridge multilevel inverter. The proposed method leverages the strengths of both techniques: SHE-PWM effectively eliminates specific low-order harmonics such as the 3rd and 5th, while SVPWM enhances voltage utilization and waveform quality by increasing the number of effective switching vectors. Simulation results in MATLAB/Simulink demonstrated the capability of the hybrid modulation scheme to significantly reduce total harmonic distortion (THD), achieving a value of approximately 1.92%, which is notably lower than conventional PWM methods. The output voltage and current waveforms were found to be nearly sinusoidal, validating the effectiveness of the proposed technique under realistic load conditions. Additionally, the approach maintains low switching frequency, improving overall inverter efficiency and reducing switching losses. The modular structure of the CHB inverter and the scalable nature of the proposed control strategy make it particularly suitable for medium to high-voltage industrial applications where power quality and efficiency are of utmost importance. Future work will focus on real-time implementation using digital signal processors (DSPs) or FPGAs, as well as experimental validation on a hardware prototype to assess the performance under dynamic and unbalanced load conditions.

### REFERENCES

- [1] J. J. Nedumgatt, D. Vijayakumar, A. Kirubakaran, and S.Umashankar, "A multilevel inverter with reduced number of switches," in Proceedings of the IEEE Students' Conference on Electrical, Electronics and Computer Science (SCEECS '12), pp.1-4, March 2012
- [2] Pratik Prajapatit, MeenakshiJayaraman "Harmonic Elimination in a Five Level Multilevel Inverter" International Conference on Computer Communication and Informatics (ICCCI -2016)
- [3] Samir Kouro, Mariusz Malinowski, K. Gopakumar "Recent Advances and Industrial Applications of Multilevel Converters" IEEE Transactions On Industrial Electronics, Vol. 57, No. 8, August 2010
- [4] S Boobalan , R.Dhanasekaran ,Hybrid Topology of Asymmetric Cascaded Multilevel Inverter with Renewable Energy Sources 2014 IEEE International Conference on Advanced Communication Control and Computing Technologies (ICACCCT).
- [5] Seyed Hossein Hosseini Ebrahim Babaei, "New cascadedmultilevel inverter topology with minimum number of switches,"Original Research Article in Energy Conversion and Management Volume 50, Issue 11, November 2009, Pages 2761-2767ELSEVIER,



**International Journal of Recent Development in Engineering and Technology**  
**Website: www.ijrdet.com (ISSN 2347-6435(Online) Volume 15, Issue 02, February 2026)**

- [6] Varsha Singh, S Gupta, S Pattnaik "New Hybrid Cascade Multilevel Inverter with Less Number of Switches" IEEE Transactions On Industrial Electronics, 2014
- [7] A. Pourdadaashnia, M. Farhadi-Kangarlu, M. Sadoughi, "Staircase Selective Harmonic Elimination in Multilevel Inverters to Achieve Wide Output Voltage Range," arXiv preprint arXiv:2104.05759, 2021.
- [8] M. Sadoughi, A. Pourdadaashnia, M. Farhadi-Kangarlu, S. Galvani, "Reducing Harmonic Distortion in a 5-Level Cascaded H-Bridge Inverter Fed by a 12-Pulse Thyristor Rectifier," arXiv preprint arXiv:2104.09642, 2021.
- [9] M. Shruthi, G. Ezhilarasan, S.M. Chandra Shekar, "Advanced SVPWM Technique for Multilevel Inverter Systems," Engineering, Technology & Applied Science Research, vol. 12, no. 3, pp. 8599–8603, 2022.
- [10] M. Wang, X. Zhang, Y. Hu, et al., "A Research on Cascaded H-Bridge Module Level Photovoltaic Inverter Based on a Switching Modulation Strategy," Energies, vol. 12, no. 10, pp. 1851, 2019.
- [11] I. H. Shanono, N. R. H. Abdullah, A. Muhammad, "A Survey of Multilevel Voltage Source Inverter Topologies, Controls, and Applications," International Journal of Power Electronics and Drive Systems, vol. 10, no. 3, pp. 1183–1199, 2019.
- [12] M. Pourdadaashnia, M. Farhadi Kangarlu, M. Sadoughi, "Staircase Selective Harmonic Elimination in Multilevel Inverters to Achieve Wide Output Voltage Range," arXiv preprint arXiv:2104.05759, 2021.
- [13] "Improved selective harmonic elimination pulse width modulation strategy in multilevel inverters," IET Power Electronics, (2011).
- [14] Bao Xin Shang, Shu Gong Zhang, Na Lei, Jing Yi Chen, "A 'nearly parametric' solution to Selective Harmonic Elimination PWM," arXiv e prints, Dec. 2015.
- [15] R. S. Kanchan, M. R. Baiju, K. K. Mohapatra, P. P. Ouseph, K. Gopakumar, "Space vector PWM signal generation for multilevel inverters using only the sampled amplitudes of reference phase voltages," IET Proceedings – Electric Power Applications, vol. 152, issue 2, 2005.
- [16] D. Lalili, E. M. Berkouk, F. Boudjema, N. Lourci, T. Taleb, "Simplified space vector PWM algorithm for five level inverter," European Physical Journal – Applied Physics, vol. 40, no. 3, Dec. 2007.
- [17] C. Victor Guzman, Carlos Sanchez, Fernando Ibanez, Julio Walter, and Maria I. Gimenez Sep. 2006, "A New Simplified Multilevel Inverter Topology for DC-AC Conversion," IEEE Trans. Power Electron vol. 21, no. 5, pp. 1311-1319,
- [18] D. Mohan, Sreejith B. Kurub "A Comparative Analysis of Multi Carrier SPWM Control Strategies using Fifteen Level Cascaded H – bridge Multilevel Inverter" International Journal of Computer Applications (0975 – 8887) Volume 41– No.21, March 2012.