International Journal of Recent Development in Engineering and Technology
Website: www.ijrdet.com (ISSN 2347 -6435 (Online)), Volume 15, Issue 11, November 2026)

Designing and Implementation of 45nm FinFET Technology

A. Anjali , D. Vineela , E. Sharoni, S .Revathi, Mrs. V. Mosherani .
(Associate Professor, ECE Department, Hyderabad Institute of Technology and management, India);
(Students,ECE Department , Hyderabad Institute of Technology and management, India)

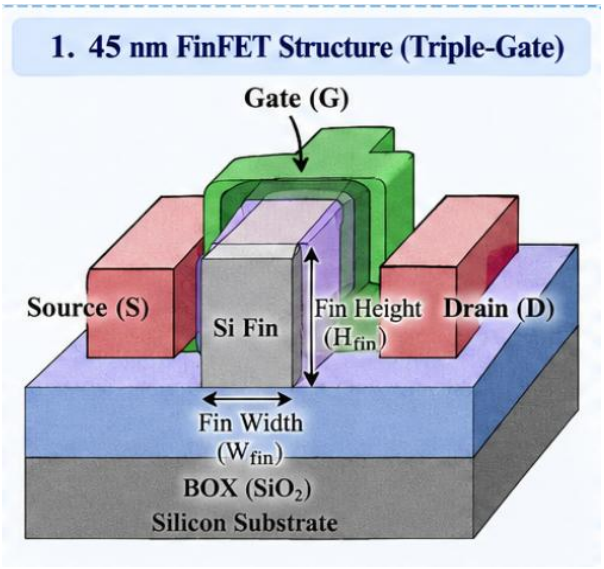
Abstract
The project focuses on the design and implementation of a 45 nm FinFET (Fin Field-Effect Transistor) technology using Xilinx. As conventional CMOS technology approaches its scaling limits, FinFET technology provides improved control over the channel and helps reduce short-channel effects, leakage current, and power consumption. In this work, a 45 nm FinFET device is designed and simulated using the Xilinx design environment to evaluate its electrical and performance characteristics. The proposed FinFET structure is analyzed based on important parameters such as drain current, threshold voltage, leakage current, power consumption, and switching characteristics. Different device configurations and bias conditions are studied to understand their impact on the overall performance. The simulation results are used to evaluate the suitability of 45 nm FinFET technology for low-power and high-performance VLSI applications. The project demonstrates the use of Xilinx tools for transistor-level design, simulation, and performance analysis. The study provides an understanding of FinFET operation and its advantages over conventional planar MOSFETs, making it useful for modern integrated circuit design.

Keywords– —45 nm FinFET, Fin Field-Effect Transistor, Xilinx Design Environment, VLSI Design, Low-Power CMOS, Short-Channel Effects, Threshold Voltage, Drain Current, Leakage Current, Power Consumption, Switching Characteristics, Device Simulation, High-Performance Integrated Circuits, Planar MOSFET, Semiconductor Technology.

I. INTRODUCTION

FinFET (Fin Field-Effect Transistor) is an advanced semiconductor technology used in modern integrated circuit design. It is developed to overcome the limitations of conventional MOSFETs, especially at smaller technology nodes. In 45 nm technology, FinFET provides improved gate control over the channel, reduces leakage current, and enhances power efficiency and device performance.

This project focuses on the design and implementation of a triple-gate FinFET using Xilinx software. Important device parameters, such as power are considered during the design process. Xilinx is used to simulate the device and analyze its electrical characteristics, including drain current, power consumption, leakage current, and switching performance. The main objective of this project is to study FinFET operation and evaluate its performance for low-power and high-performance integrated circuit applications.



II. AIM AND OBJECTIVE

2.1 AIM

The aim of this project is to design and simulate a 45 nm FinFET-based digital circuit using Verilog HDL in the Xilinx Vivado environment. The project focuses on understanding the basic principles of FinFET technology and its advantages over conventional planar MOSFETs, including improved channel control, reduced leakage, and enhanced switching performance. The designed circuit is verified through RTL simulation to ensure correct functional behavior.

International Journal of Recent Development in Engineering and Technology
Website: www.ijrdet.com (ISSN 2347 -6435 (Online)), Volume 15, Issue 11, November 2026)

Furthermore, synthesis, implementation, and available power estimation features are explored to evaluate the circuit's implementation characteristics and estimated power consumption, providing an introductory understanding of digital VLSI design and low-power integrated circuit development.

OBJECTIVE

The main objectives of this project are to study 45 nm FinFET technology, understand its benefits, and develop a simple digital circuit using Verilog HDL. The design is simulated in Xilinx Vivado using a testbench to verify its functional correctness under different input conditions.

The project also aims to perform synthesis, generate a gate-level netlist, and implement the design on a supported target device. Additionally, power analysis is performed to examine estimated dynamic power, static power, and total power consumption. Finally, the obtained simulation and implementation results are analyzed and documented to understand digital circuit performance and power estimation techniques.

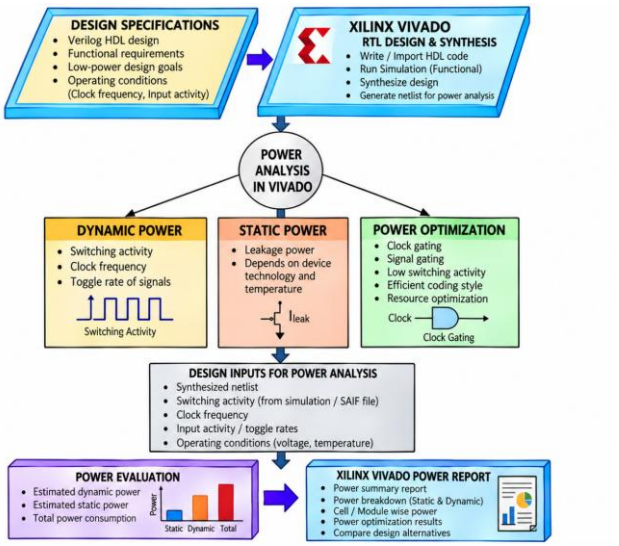
III. COMPONENTS

The components used in the proposed system are;

3.1 Software Requirements

Xilinx Software:
Xilinx is a software and hardware development ecosystem used to design, simulate, synthesize, implement, and test digital circuits on FPGA devices. It is widely used in Electronics and Communication Engineering (ECE), VLSI design, digital electronics, embedded systems, and hardware verification. For your project on 45 nm Triple-Gate FinFET technology, Xilinx can help you implement and test digital logic written in Verilog HDL.

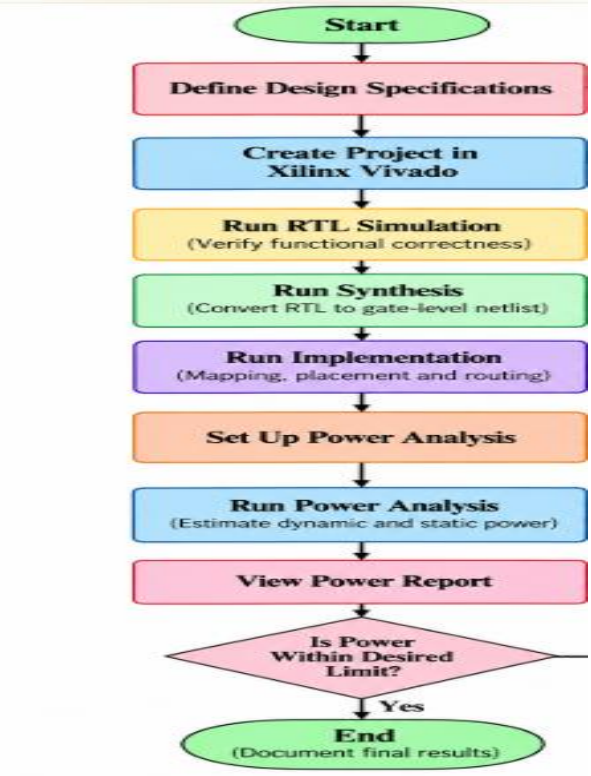
IV. BLOCK DIAGRAM



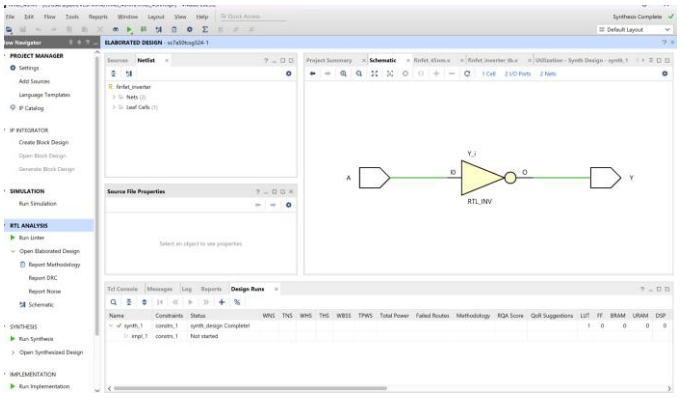
V. WORKING PRINCIPLE

The proposed system focuses on analyzing and reducing the power consumption of a digital circuit using Xilinx Vivado software. Initially, the design specifications are defined, including Verilog HDL code, functional requirements voltage, and temperature. Next, the design is created in Xilinx Vivado using RTL design techniques, followed by synthesis to convert the RTL code into a gate-level netlist. The synthesized design then undergoes implementation, which includes technology mapping, placement and routing. After implementation, power analysis is performed to estimate dynamic power and static power. Dynamic power depends on switching activity, clock frequency, voltage, and capacitance, whereas static power is mainly associated with leakage current. The software then generates a power report containing estimated total power consumption and its dynamic and static components. Based on the report, power optimization techniques such as reducing unnecessary switching activity, optimizing logic, and using clock-enable techniques can be applied. The modified design is analyzed again to compare the power estimates and determine whether the design meets the desired power target. Finally, the results are documented to evaluate the effectiveness of the power optimization process.

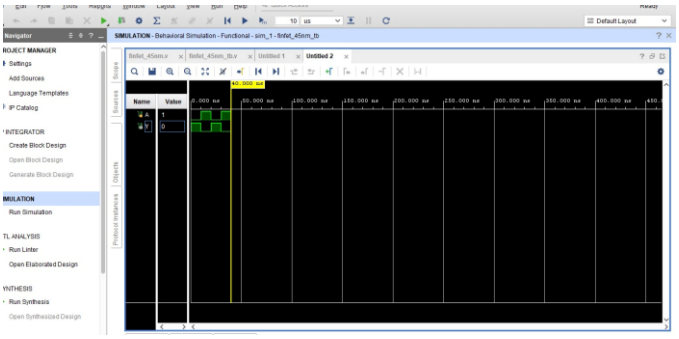
International Journal of Recent Development in Engineering and Technology
Website: www.ijrdet.com (ISSN 2347 -6435 (Online)), Volume 15, Issue 11, November 2026)

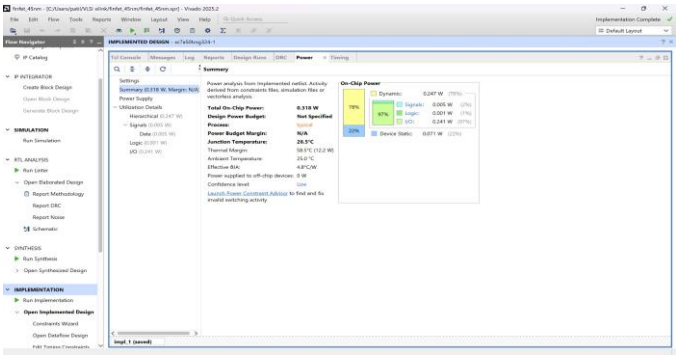


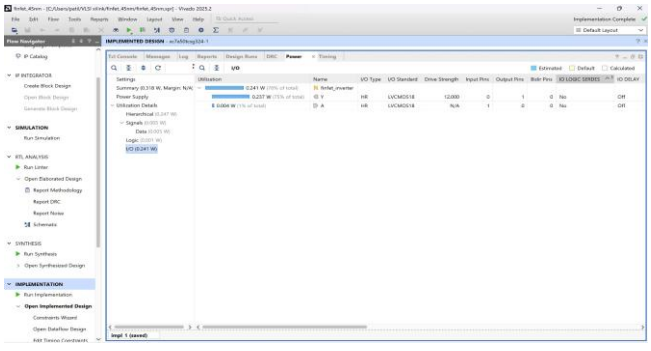
VI. CIRCUIT DIAGRAM



VII. RESULT







International Journal of Recent Development in Engineering and Technology
Website: www.ijrdet.com (ISSN 2347 -6435 (Online)), Volume 15, Issue 11, November 2026)

Comparison of MOSFET and Triple-Gate FinFET Power Consumption			
S. No.	Parameter	MOSFET	Triple-Gate FinFET
1	Total Power Consumption	0.350 W*	0.318 W
2	Power in milliwatts	350 mW*	318 mW
3	Power Difference	—	32 mW lower
4	Power Reduction	—	9.14%*

VIII. ADVANTAGES

- **Enhanced Electrostatic Control:** Improves control of the transistor channel.
- **Lower Heat Generation:** Reduced power dissipation can help limit heat generation.
- **Better Signal Integrity:** Stable switching can support reliable circuit operation.
- **Scalable Architecture:** Provides a foundation for studying advanced transistor designs.
- **Efficient Circuit Operation:** Supports analysis of switching behavior and power requirements.
- **Design Optimization**: Device parameters can be adjusted to study performance improvements.

IX. APPLICATIONS

- **Low-Power Processors:** Used in processor designs to improve power efficiency.
- **Mobile Devices:** Applied in smartphones and tablets to support energy-efficient operation.
- **High-Performance Computing:** Used in computing circuits that require high speed and efficient operation.
- **Memory Circuits:** Applied in semiconductor memory and associated logic circuits.
- **Consumer Electronics:** Applied in electronic devices such as smart TVs, digital cameras, and multimedia systems.
- **Communication Systems:** Used in digital signal-processing and communication integrated circuits.

X. CONCLUSION

The project focuses on the design and implementation of 45 nm Triple-Gate FinFET technology. The structure provides improved gate control and has the potential to reduce short-channel effects and leakage current. The study helps explain the importance of transistor structure and device parameters for low-power and high-performance applications.

XI. FUTURE SCOPE

1. Power Optimization: Reduce overall power consumption using suitable low-power design techniques.
2. Leakage Reduction: Investigate methods to minimize leakage current in Triple-Gate FinFET devices.
3. Performance Improvement: Improve switching speed and circuit performance.
4. MOSFET Comparison: Compare MOSFET and Triple-Gate FinFET designs under identical operating conditions.

REFERENCE

1. Karimi, K., Fardoost, A., and Javanmard, M. (2024). "Comprehensive Review of FinFET Technology: History, Structure, Challenges, Innovations, and Emerging Sensing Applications." *Micromachines*, 15(10), 1187. https://doi.org/10.3390/mi15101187
2. Yadav, N., Khandelwal, S., and Akashe, S. (2013). "Analysis of Conventional CMOS and FinFET Based 6-T XOR-XNOR Circuit at 45nm Technology." *International Journal of Computer Applications*, 84(4), 4–9. https://doi.org/10.5120/14562-2670
3. Bhattacharya, D., and Jha, N. K. (2014). "FinFETs: From Devices to Architectures." *Advances in Electronics*, 2014, Article ID 365689. https://doi.org/10.1155/2014/365689
4. Maurya, R. K., and Bhowmick, B. (2022). "Review of FinFET Devices and Perspective on Circuit Design Challenges." *Silicon*, 14, 5783–5791. https://doi.org/10.1007/s12633-021-01366-z
5. AMD Xilinx. *Vivado Design Suite User Documentation*. Available at: https://docs.amd.com/