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Review of High-Performance Polar Encoding-Decoding Systems

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***Abstract*— Polar codes, introduced by Erdal Arıkan in 2009, have become one of the most significant breakthroughs in channel coding theory due to their capacity-achieving nature and efficient implementation potential. This review focuses on recent advancements in high-performance polar encoding and decoding systems, with emphasis on their architectural innovations, algorithmic improvements, and hardware optimizations for real-time applications. Special attention is given to successive cancellation (SC), successive cancellation list (SCL), belief propagation (BP), and hybrid decoding strategies, which significantly enhance performance in terms of latency, throughput, and energy efficiency. The review also highlights practical deployment challenges and discusses how polar codes are being integrated into modern communication standards such as 5G.**

Keywords*— *VLSI, Polar, Encoding, Decoding, 5G.

I. INTRODUCTION

Error correction coding plays a crucial role in modern digital communication systems, enabling reliable data transmission over noisy channels. Among various coding techniques, polar codes have emerged as a revolutionary solution due to their ability to achieve channel capacity with low-complexity encoding and decoding [1]. Proposed by Erdal Arıkan, polar codes are the first class of codes proven to achieve the symmetric capacity of binary-input discrete memoryless channels under a low-complexity successive cancellation (SC) decoder. The introduction of polar codes marked a paradigm shift in coding theory, leading to intensive research in both theoretical and practical aspects of their implementation [2].

The significance of polar codes grew even further when they were adopted as part of the 5G New Radio (NR) standard for control channel communications by the 3rd Generation Partnership Project (3GPP) [3]. This integration brought forth a new wave of interest in enhancing the performance of polar coding systems, especially to meet the stringent requirements of latency, throughput, and power efficiency in real-world applications. To achieve high performance, researchers have explored multiple variations and optimizations in polar encoding and decoding mechanisms. Techniques such as successive cancellation list (SCL) decoding, belief propagation (BP), and hybrid decoding architectures have demonstrated promising improvements in error correction performance and hardware efficiency [4].

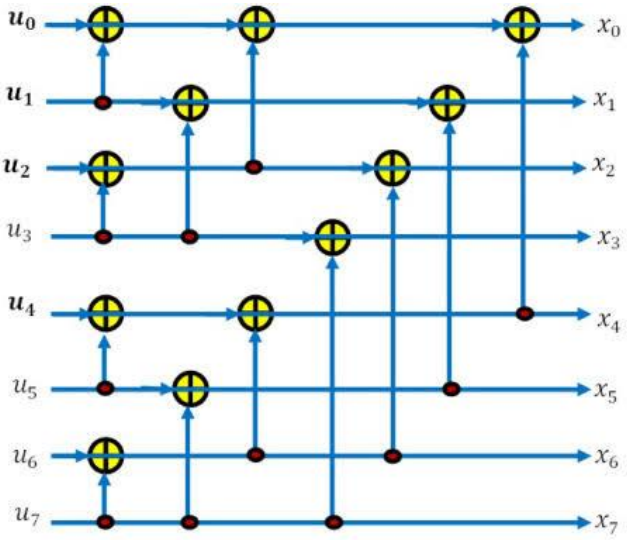

Figure 1: Polar Codr

On the encoding front, polar codes are inherently structured using a recursive construction of a generator matrix based on the Kronecker product. This deterministic nature of polar encoding simplifies its implementation; however, efficient parallelism and reduced latency are essential to match modern system demands [5]. Therefore, parallel and pipelined encoder architectures have been developed to support high-speed transmission environments. Likewise, decoding strategies have evolved from simple SC to SCL with CRC-aided enhancements, delivering significant performance gains especially in short to moderate code lengths where SC decoding falls short [6].

This review aims to consolidate current research trends and advancements in high-performance polar encoding-decoding systems. It systematically explores algorithmic developments, architectural designs, hardware implementation strategies, and optimization techniques. Furthermore, it discusses comparative evaluations across different decoders and provides insights into real-world challenges faced during integration into modern communication systems. Finally, the review outlines future directions that could guide upcoming innovations in the design of polar code systems for next-generation networks, particularly beyond 5G.

II. LITERATURE SURVEY

In 2015, Sarkis et al. introduced flexible and low-complexity encoding and decoding methods for systematic polar codes. Their approach allowed for hardware and software implementations that could adapt to various code lengths and rates without significant overhead. This flexibility was crucial for applications requiring dynamic code configurations, paving the way for more adaptable communication systems [1].

The 2016 study by Yuan and Parhi focused on the architecture and optimization of high-throughput belief propagation (BP) decoding of polar codes. They explored parallel BP decoder designs, analyzing silicon area, throughput, and power consumption. Innovations like adaptive quantization and early convergence detection were introduced to enhance error-correcting performance and throughput [2].

Cammerer et al. in 2017 proposed scaling deep learning-based decoding of polar codes via partitioning. By dividing the encoding graph into smaller sub-blocks and training them individually, they achieved near-optimal performance per sub-block. This method allowed for high parallelization and competitive bit error rate (BER) performance, marking a significant step in combining deep learning with polar code decoding [3].

In 2018, Fan et al. addressed the latency challenges in list successive-cancellation decoding (LSCD) for polar codes. They introduced a selective expansion method and a double thresholding scheme to reduce computation and latency. Their VLSI architecture, implemented using UMC 90 nm CMOS technology, achieved a decoding throughput of 460 Mbps at a clock frequency of 658 MHz, demonstrating significant improvements in latency and hardware efficiency [4].

The 2019 study by Doan et al. explored optimizing polar codes compatible with off-the-shelf low-density parity-check (LDPC) decoders. By jointly designing the polar code and the parity-check matrix, they closed the performance gap between LDPC-style decoding and Arıkan's BP decoding. This approach allowed polar codes to achieve similar error-rate performance compared to standardized LDPC codes, especially in high SNR regions [5].

Xu et al. in 2020 presented a deep learning-aided belief propagation decoder for polar codes. Their approach leveraged neural networks to enhance the decoding process, resulting in improved error-correcting performance and faster convergence. This integration of deep learning techniques into polar decoding algorithms marked a significant advancement in the field [6].

In 2021, a study by T., Hoydis focused on developing hardware-efficient polar decoders tailored for 5G Internet of Things (IoT) communications. By employing a modified semi-parallel decoder architecture with 4-bit decoding algorithms and a look-ahead approach, the design achieved significant reductions in latency and improved hardware resource utilization. This advancement was crucial for real-time and high-quality applications in resource-constrained IoT scenarios [7].

The 2022 research by Giard et al. delved into low-latency software polar decoders. By exploiting modern processor capabilities and adapting algorithms at various levels, they achieved significant improvements in latency and throughput. Their proposed decoders were suitable for high-performance software-defined radio applications, offering lower latency and memory footprint compared to existing solutions [8].

Rezaei et al. in 2023 proposed unrolled architectures for high-throughput encoding of multi-kernel polar codes. Their design supported various kernel combinations, offering flexibility in code construction. The FPGA implementation demonstrated a throughput of 1080 Gbps for a code size of N=4096, showcasing the potential for ultra-high-speed polar encoding in next-generation communication systems [9].

The 2024 study by Devadoss et al. introduced a fully parallel low-density parity-check (LDPC) code-based polar decoder

architecture for 5G wireless communications. By applying pruning techniques and pipelining in check node and variable node architectures, they achieved a throughput of 2.44 Gbps. The design demonstrated superior error-correcting performance and hardware efficiency, making it a suitable alternative to existing decoders in 5G systems [10].

III. CHALLENGES

Challenges in High-Performance Polar Encoding-Decoding Systems

1. **Latency and Throughput Trade-off** While polar codes offer excellent error-correction performance, their standard successive cancellation (SC) and list-SC decoding methods are inherently serial in nature, resulting in high latency. High-throughput designs often require deep pipelining or unrolled architectures, which come at the cost of increased hardware complexity and resource usage.
2. **Hardware Complexity in List Decoding** List successive cancellation decoding (LSCD), a performance-enhancing technique, significantly improves decoding accuracy but introduces high memory and logic complexity due to path metric computations and sorting operations. This makes hardware implementation resource-intensive, particularly for large block lengths.
3. **Scalability and Flexibility** Supporting multiple code lengths and rates in a single decoder architecture remains a challenge. Most hardware-optimized decoders are rigid and tailored for specific configurations, limiting adaptability in multi-standard environments like 5G and beyond.
4. **Memory Bottlenecks** Polar decoders often require multiple stages of intermediate data storage, especially in belief propagation and LSCD. Memory access becomes a bottleneck, impacting both speed and power consumption, particularly in resource-constrained environments such as IoT.
5. **Energy Efficiency for IoT and Mobile Devices** Implementing high-performance polar decoders in low-power applications, such as IoT or mobile devices, is challenging. Optimizing for energy efficiency while maintaining error correction performance and speed is still an ongoing area of research.
6. **Decoder Parallelism Limitations** Unlike LDPC and Turbo codes, polar codes exhibit decoding dependency across bit positions, which limits the extent of parallelization achievable in SC and LSCD algorithms. While belief propagation offers parallelism, it sacrifices error performance.
7. **Error Floor Phenomenon** Some high-speed polar decoders, especially those using approximations or aggressive quantization, exhibit error floors at high SNR, limiting their application in mission-critical or ultra-reliable low-latency communication (URLLC) systems.
8. **Design for 5G and Beyond** As polar codes are used in 5G for control channels, meeting the stringent latency and reliability requirements while keeping hardware overhead low is still a bottleneck. Decoders must be tightly integrated with existing 5G modems, requiring extensive optimization.

IV. CONCLUSION

High-performance polar encoding-decoding systems have emerged as a promising solution for modern communication standards due to their capacity-approaching performance and suitability for 5G networks. However, numerous challenges persist, including high latency, limited parallelism, increased hardware complexity, memory bottlenecks, and the difficulty of achieving energy efficiency in constrained environments. Despite these hurdles, ongoing advancements in decoder architectures, deep learning integration, and flexible code designs continue to push the boundaries of performance. Addressing these challenges holistically will be critical to fully harness the potential of polar codes in next-generation communication systems.

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