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Review of Low Voltage 6T SRAM Cell Design and Analysis

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***Abstract*— SRAM has become a major component in many VLSI Chips due to their large storage density and small access time. SRAM has become the topic of substantial research due to the rapid development for low power, low voltage memory design during recent years due to increase demand for notebooks, laptops, IC memory cards and hand-held communication devices. SRAMs are widely used for mobile applications as both on chip and off chip memories, because of their ease of use and low standby leakage. This paper discusses many SRAM factors, including Static Noise Margin (SNM), Read Access Time (RAT), Write Access Time (WAT), Read Stability and Write Ability, Power, Data Retention Voltage (DRV), and Process Control. All these factors are crucial when designing SRAM.**

Keywords*— *Low power SRAM, SRAM factor, low delay and power, read and write.

I. INTRODUCTION

6T static random-access memory is a type of semiconductor memory that uses bitable latching circuitry to store each bit. The term static differentiates it from dynamic RAM which must be periodically refreshed. SRAM exhibits data remembrance, but is still volatile in conventional sense, that data is eventually lost when memory is not powered.

CMOS devices have been scaled down in order to achieve higher speed, performance and lower power consumption [1]. SRAM means Static Random Access Memory. The SRAM cell that we considered in this paper was 6T SRAM cell which consists of two crossly coupled inverters and access transistors to read and write the data. In case of the SRAM cell the memory built is being stored around the two cross coupled inverters. If we consider that, the input to the first inverter is logic 1 then the output of this inverter will be logic 0. So, after one cycle the output of second inverter will be logic 1. From this we can say that as long as the power is supplied to the SRAM cell logic 1 will be circulated in the inverters. Hence there is no need for periodic refreshing of the circuit. Where as in DRAM the circuit need to be refreshed periodically [2]. SRAM technology is most preferable because of its speed and robustness [3]. Therefore, SRAM is much faster when compared with the DRAM.

II. 6T SRAM CELL OPERATION

Standby Mode (the circuit is idle) In standby mode word line is not asserted (word line=0), so pass transistors N3 and N4 which connect 6t cell from bit lines are turned off. It means that cell cannot be accessed. The two cross coupled inverters formed by N1-N2 will continue to feedback each other as long as they are connected to the supply, and data will hold in the latch.

2. Read Mode (the data has been requested) In read mode word line is asserted (word line=1), Word line enables both the access transistor which will connect cell from the bit lines. Now values stored in nodes (node a and b) are transferred to the bit lines. Assume that 1 is stored at node a so bit line bar will discharge through the driver transistor (N1) and the bit line will be pull up through the Load transistors (P1) toward VDD, a logical 1. Design of SRAM cell requires read stability (do not disturb data when reading).

3. Write Mode (updating the contents) Assume that the cell is originally storing a 1 and we wish to write a 0. To do this, the bit line is lowered to 0V and bit bar is raised to VDD, and cell is selected by raising the word line to VDD.

Typically, each of the inverters is designed so that PMOS and NMOS are matched, thus inverter threshold is kept at VDD/2. If we wish to write 0 at node a, N3 operates in saturation. Initially, its source voltage is 1. Drain terminal of N2 is initially at 1 which is pulled down by N3 because access transistor N3 is stronger than N1. Now N2 turns on and P1 turns off, thus new value has been written which forces bit line lowered to 0V and bit bar to VDD. SRAM to operate in write mode must have writeability which is minimum bit line voltage required to flip the state of the cell.

III. LITERATURE REVIEW

An improvement provided in SRAM depends on either of the three parameters or combination of transistor count, connection method and technology used. As VLSI suggests, the improvement expected should be in the form of reduction of power, area and delay. It can be done in 2 ways, (i) Reduction of one parameter without any changes in other 2 parameters or (ii) Reduction of two parameters with sacrificing changes occur in the other parameter. Various

methods are already available to reduce area power and delay like, sleep transistor, tail transistor, power gate method, separation of read and write operations, conducting PMOS technique, less supply voltage method.

[1] In this paper, they used Cadence Virtuoso to perform an extensive investigation of the design of the 6T SRAM memory cells implemented in 45nm and 90nm cmos technologies. Through the creation and examination of test circuits and schematics, the complex internal workings of the 6T SRAM were examined. When different input values were used, responses, including Transient, were produced. Furthermore, we meticulously calculated important characteristics like average power usage, area and circuit delay. there were significant variations in the 6T SRAM performance between the three methods. In particular, the average power, area and latency in 45nm technology were better than those in 180nm and 90nm technology. 6T SRAM's layout was painstakingly created for 45nm and 90nm technology. Thorough rule checks and layout against schematic verifications were carried out, yielding insightful information on the Cadence tool.

[2] The proposed 10T SRAM has write energy and leakage power reduction of 89% and 96.6%, respectively while maintaining a similar read enery as compared to 9T SRAM. Additionally, a 4 Kb SRAM array based on 10T SRAM is implemented in 180- nm SCL technology to analyze the suggested IMC architecture. At 1.8 V, 60 MHz, the suggested IMC architecture achieves energy efficiency of 0.43 TOPS/W for 1-bit logic and 0.41TOPS/W for 1-bit addition. The area efficiency of 65.2% for a 136 32 array is achieved. The energy-efficient 10T SRAM bit cell with enhanced write stability is proposed for normal operation and InMemory Boolean based computation. The proposed 10T SRAM bit cell offers 40 % higher WSNM, 89% lesser write energy and 96.6% lower leakage power with nearly same RSNM when compare to 9T SRAM at 1.8V supply voltage. A 4Kb SRAM array based IMC architecture is fabricated by using SCL 180nm technology. At 60 MHz, the proposed IMC architecture is performed for arithmetic and logic operation.

[3] The proposed MTCMOS 8T SRAM cell is implemented, analyzed, verified and compared to the existing SRAM cells using Cadence Virtuoso with a channel length of 45 nm at a power supply of 500 mV. In proposed MTCMOS 8T SRAM cell, i) read stability RSVNM is increased by 5.89%, 5.72% and 4.74% ii) write stability WTV is increased by 4.16%, 4.16% and 5.05% iii) hold stability HSNM is increased by 0.24% iv) power consumption is decreased by 58.87%, 3.164%

and 66.49% in comparison to conventional 6T, existing 8T and existing 9T SRAM cell respectively v) overall read path leakage current is reduced by 94.83% and 87.420%, when compared with existing 8T and existing 9T SRAM cell respectively.

[4] In this paper, we focus on power optimization analysis of different SRAM cells using transistor stacking technique. Using this stacking technique, instead of using single size transistor, we use two half size transistors. Here we connect the transistors in series which are turned off. This reduces the leakage current which in turn reduces the power consumption of SRAM cell. In this paper power consumption is analyzed for various SRAM cells with and without stacking technique using at different voltages are simulated using Hspice-A 2008.03 tool.

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[5] In this paper, stability analysis of conventional 6-T SRAM cell and Schmitt trigger (ST) based 10-T SRAM cell with optimized sizing parameters has been performed and compared. The read stability, write ability, delay and dissipated power have been investigated. By using N-curve methodology a significant improvement of 4.49%, 5.13% and 28.65% in SVNM, SINM and WTI respectively was observed for Schmitt trigger (ST) based 10-T SRAM cell as compared to optimized 6T SRAM cell. Furthermore, the effects of supply voltage and temperature on conventional 6T SRAM stability in read and write operational mode have also been examined. Furthermore, both read delay and read current were investigated for ST based 10-T SRAM cell and found in desirable limits. It is also interesting to note that read delay is improved by 66%. Monte-Carlo simulation of the ST based 10-T SRAM cell circuit is carried out in order to find the deviation for power and the read current. The read current of the 10T topology is found to be 29.97µA with standard deviation of 4.55µA. Mean dynamic power for all process corners is also calculated by monte-carlo simulation of 4000 point each and deviation from the mean power was obtained. For simulation process 90nm technology node at 1V power supply was used on cadence virtuoso tool.

IV. IMPROVING THE 6T SRAM

This review find improving the 6T SRAM circuit's performance by using Low-Voltage Transistors instead of conventional transistors and reduced the width of the transistors when compared to [4]. This modification's main goal is to maximize the circuit's write operations while utilizing Low-Voltage Transistors benefits, which include a lower threshold voltage and increased efficiency at lower power supply voltages. The write process has been thoroughly studied and modified to take advantage of the unique advantages of LVT transistors and reducing the width of the transistors, with a focus on decreasing write latency, improving overall write power and reduce the area. The circuit's routing and layout have been methodically redesigned to accommodate the special qualities of LVT transistors, with an emphasis on reducing resistance and parasitic capacitance to improve overall performance. The suggested methodology is verified through micro wind software.

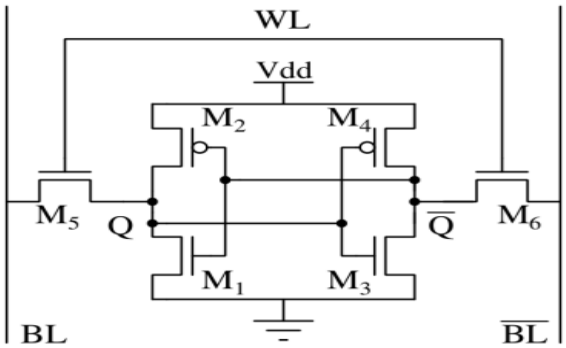

Fig:1 6T SRAM

Conventionally, elementary constituent of memory devices is Six Transistor (6T) SRAM cell as shown in Fig. 1. It involves two back to back connected inverters (M1, M3) and (M2, M4) forming a latch to keep the data intact. The access transistors M5 and M6 are utilized to achieve read and write operations. The access transistors are activated using word line connected with gate. Using common path i.e. (M5, M6) for read and write leads to conflicting situation in read stability and writability of the cell. For read process, the pulldown transistors and access transistors are responsible. Cell ratio CR = Wpd Wac is defined as ratio of width of pull-down transistor to the width of access transistor. The RSNM is explained in terms of CR i.e. width of M1 w.r.t M5 and required to be kept high to uphold good read operation. While the lower pull-up ratio CR = Wpu Wac is desirable to enhance writability of SRAM cell. However, if access transistor is strengthened beyond a certain limit to decline PR, it may result is destructive read also. Furthermore, during standby mode, to ensure maximum HSNM identical strength of pull up and pull-down transistors is required to set the trip point of both inverters at Vdd/2. Consequently, it is a challenge to propose some modification in bit cell topology to retain read stability and write ability while reducing the consumed power. This can be concluded from Eqn. that to reduce total power while read and write process, diminution of supply voltage becomes an essential condition. Though, scaling down supply voltage effects noise margins as well as delay in various process corners. Specifically, lower level voltage during read operation become difficult to maintain in SF process corner. This is because of higher strength of fast PMOS in contrast with slow NMOS with same size restraints. To settle the CR

and PR values to maintain balance between read and write noise margins the width of transistors is enhanced. Conventionally pull-down transistors are kept strongest to improve conductivity while read cycle. But this also leads to increase in leakage current during standby mode. Threshold voltage of transistor also increases with increment in width due to inverse narrow width effect. Though, this increase in Vth is not adequate to contain the rise in leakage current.

The results for the 6T SRAM are achieved utilizing 45nm with the given supply voltage. Figure 3 shows waveforms with a pulse width of 25 ns and a period of 50 ns, which are obtained by taking the values of VDC for VDD=1 v, VPULSE for BL=1 v to 0 v, and BL BAR=0 v to 1 v. The term line ascends. The waveforms show Q and Q BAR as the output and PB, BL BAR, and WL as the input. Bit lines BL BAR and b must complement one another. The data are saved at Q and Q BAR, and the read or write operation is dependent upon the input supplied at BL and BL BAR. The application of the same procedure and its values in 45nm technology.

V. CONCLUSION

The exact objectives, goals, and performance criteria of the design would determine the outcomes for a 6T SRAM cell developed using Cadence Virtuoso software in multiple technologies employing 180nm, 45nm, and 90nm. However, the following broad conclusions can be based on. Stability is a 6T SRAM cell intended to keep data storage steady. By utilizing the feedback loop, its cross-coupled inverter pair assures the storage of an illogical value. The process of implementing using Cadence Virtuoso validates the cell's stability, reducing the possibility of data loss or modification. Operations for Read and Write: The 6T SRAM cell enables quick read and write procedures. The access transistors make it possible to read the data from storage without significantly altering the state of the cell. The write transistors also make it possible to change the data that has been saved without interfering with other cells in the array. Noise Margin: Cadence Virtuoso's implementation enables examination of the noise margin, a metric for the SRAM cell's resistance to noise. An improved capacity to withstand outside forces without making mistakes is indicated by a greater noise margin. The design may be made more reliable by optimizing it to provide a reasonable noise buffer.

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