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VLSI Implementation of Advanced Microcontroller Bus Architecture-Advanced High Performance Bus (AMBA-AHB) Protocol

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***Abstract*— AHB is generally a high performance bus which can provide better bandwidth operation. Through AHB, a design can achieve features like split transactions, better data bus configuration, burst transfer, single clock edge operation etc. AHB is used on ARM7, ARM Cortex-M and ARM9 based designs. AHB system design contains AHB master, AHB Slave, AHB Decoder and AHB arbiter. This paper presents VLSI implementation of Advanced Microcontroller Bus Architecture-Advanced High Performance Bus (AMBA-AHB) protocol.**

***Keywords*—AHB, AMBA, VLSI, Microcontroller, Bus, ARM, Speed.**

I. INTRODUCTION

AMBA was first presented by ARM in the year 1996. The Advanced System Bus (ASB) and the Advanced Peripheral Bus were the first AMBA buses that were developed (APB). ARM introduced the AMBA High-performance Bus (AHB), which is a single clock-edge interface, in its second version, AMBA 2, which was released in 1999. AMBA 3, which included the Advanced eXtensible Interface (AXI) to provide even better performance connection and the Advanced Tracing Bus (ATB) as part of the CoreSight on-chip debug and trace solution, was launched by ARM in the year 2003. AMBA stands for Advanced Micro Device Bus Architecture.

The acronym "Advanced Peripheral Bus" (APB) refers to a component of the "Advanced Microcontroller Bus Architecture" (AMBA) family of standards. It is a simple interface, and the layout is to enhance the design in order to decrease the amount of power that is used and the amount of uncertainty that is present in the interface. In contrast to AHB, it is a Non-Pipelined convention, and it is used to link peripherals with the SoC that have a limited data transmission capacity [1]. In the field of semiconductor manufacturing, the Advanced Microcontroller Bus Architecture (AMBA) offered from ARM is among the industry standards that is used the most often for the construction of System on Chip (SoC).

When it comes to the design of high-performance chipsets, adhering to the AMBA requirements offers a variety of benefits, including right-first-time development and independence from particular technologies [2]. AMBA, which stands for advanced microcontroller bus architecture, has developed to the point that its standards now extend far beyond microcontrollers.

This work implements AMBA, which stands for Advanced Microcontroller Bus Architecture, as well as ASB APB, which stands for Advanced System Bus and Advanced Peripheral Bus. The purpose of the study that has been presented is to synthesise and model the complicated interaction that exists between AMBA ASB and APB. Verilog language with finite state machine models built in ModelSim Version 10.3 and Xilinx-ISE design suite, version 13.4 is used to extract synthesis, design usage summary, and power reports. This technique was chosen for the requested task and was implemented using Verilog language. The APB Bridge, arbiter, and decoder are all developed in preparation for their deployment. The AMBA ASB APB module is where the master establishes communication with the APB bus. The arbiter first assesses the condition of the master and its priority, and then it begins interacting with the bus [6].

II. BACKGROUND

P. Jain et al.,[1] The Verilog programming language and Verilog Testbench are being used by the system that has been adopted for the suggested task. This is done in order to extract synthesis and design utilisation summaries. Verilog programming was used in the design, which significantly increased the reusability of the Testbench components, such as the creation of Tasks for a variety of different test scenarios. Suresh A. et al. [2], The Advanced Highperformance Bus (AHB) and the Advanced peripheral Bus are the two protocols that are receiving the most of the attention during this effort (APB). We want to build an AMBA AHB-APB bridge from Register Transfer Level (RTL) to Graphical Display System (GDSII) using solely open source tools and libraries.

While developing this bridge, we will keep in mind that these requirements constitute an open standard.

N. Gaikwad et al.,[3] In a world that is constantly evolving, where new intellectual property (IP) and chips are developed every day with shorter time to market, the creation of a highly strong verification mechanism within a short period of time is a key demand of the rapidly expanding VLSI sector. The system-on-a-chip, or SoC, design became the primary integrated methodology for minimising the amount of time needed to design a complete system after the introduction of a standardised signal bus architecture. This architecture is used for the interconnection of the various modules that make up a system. K. Rudnicki [4] offer an intellectual property core of a coprocessor that is capable of handling calculations that need integer multiple-precision arithmetic (MPA). There are still applications that demand more numerical precision, despite the fact that normal 32-bit and 64-bit arithmetic is adequate to tackle many of the computational challenges that arise. As a result, the objective of the coprocessor that was designed is to assist and unload the central processing unit (CPU) in calculations of this kind. The newly designed digital circuit of the coprocessor operates with integer values that have a precision that is close to 32 kbits at their most extreme.

N. Pravin et al.,[5] This study describes an implementation of the Fourier Segmentation process that is used in the Empirical Wavelet Transform that is based on the utilisation of Field Programmable Gate Arrays (FPGAs). The Empirical Wavelet Transform is a technique that may be used to ascertain the modes of a particular signal by constructing wavelets that are customised to the signal that is being processed. K. Rawat et al.,[6] The decoder makes use of the correct address lines in order to pick a bus slave, and the slave provides an acknowledgment to the bus master when the selection has been made. Within the outcome portion of the study, an RTL perspective as well as an extracted design overview of an AMBA ASB APB module at system on chip are shown. The amount of power used by SoC architectures is brought into focus by the increasing complexity of their designs. There are several different power components, each of which contributes to the total power consumption that is derived from the power reports. Hence, power reports provide designers with a better grasp of the power use they are responsible for. The overall power used by the clocks in the proposed architecture is 0.66 milliwatts, while the total power consumed by the hierarchy is 1.05 milliwatts, while the total logical power consumed by the hierarchy is 0.30 milliwatts, and the total signal power consumed by the hierarchy is 0.74 milliwatts.

A graph is also displayed in order to facilitate clear comprehension of the distribution of powers.

J. Chhikara et al.,[7] Each and every design unit is made up of a collection of smaller functional pieces that are referred to as modules or subsystems. It is essential for the proper operation of the system that various modules communicate with one another and pool their respective resources. The issue arises when one component of the system uses a different protocol than the rest. Every module has its own unique bit rate or baud rate of data transmission, which may be synchronous or asynchronous depending on the needs of the application. This work provides a description of an architecture that outlines how the data may be transferred from one protocol to another protocol. It does this by taking use of I2C's flexible protocols, which enables it to be compatible with the APB AMBA protocol. K. Rawat et al.,[8] In this study, one of AMBA (Advanced Microcontroller Bus Architecture) is built. It is known as AMBA APB (Advanced Peripheral Bus), and it offers the lowest possible power consumption together with the lowest possible bandwidth. In order to do this, a Verilog-based implementation of an APB Bridge with Reset Controller design was carried out. Under the circumstances of Power-on Reset (POReset), the Reset controller will introduce a reset signal known as BnRES. This will allow for the elimination of the propagation of metastable values and the prevention of glitches. The power report demonstrates that a number of different power components contribute to the overall amount of power that is used by the APB bridge design.

E. Karimi et al. [9] provide a novel failure model that use a graph model for the purpose of evaluating conventional On-Chip buses. This approach will be improved so that testing may be completed more quickly. Utilizing AMBA-AHB as the experimental result, the suggested fault model demonstrates efficiency when compared with the testing for similar stuck-at faults. Cheng-Ta Wu et al.,[10] Since the design of SoCs is becoming more intricate, the ability to reuse IPs (intellectual property) is becoming an increasingly important factor in efforts to reduce the amount of time needed for the creation and integration of embedded systems. Nevertheless, the ability to reuse the IPs will be impacted in various ways depending on the SoC design environment, such as in different system buses. As part of this project, a standardised OCP-AHB bus wrapper was developed and deployed.

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III. METHODOLOGY

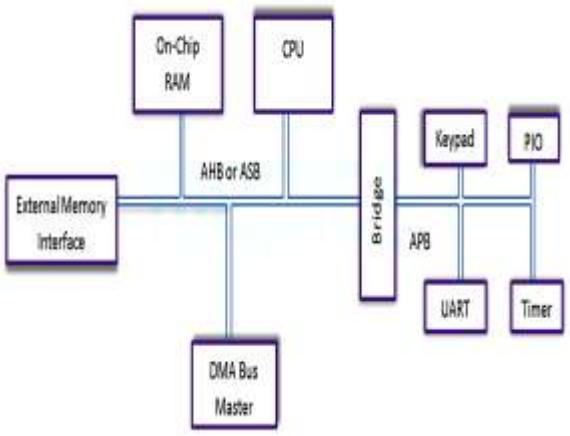

Figure 1: Work flow

As a high performance pipelined bus, ASB can be used in the design of many embedded microcontrollers. It supports the connection of many processors, external memory interfaces and on-chip memories. The main features like burst transfer, multiple bus master support and better pipelined operation can be obtained through ASB.

The main components of ASB are ASB Master, ASB Slave, ASB Arbiter and ASB Decoder. ASB Master initiates the write and read operations through address and control information. Many bus masters are present in ASB; but at a time only one of them will get access. ASB Arbiter will help the master to achieve access to ASB. The main function of ASB Slave is to respond to the read and write operations. For decoding the address and to select the appropriate slaves ASB Decoder is used.

Non-Sequential, Sequential and Address-only are the three main types of transfer that can take place through ASB. The different signals used in this bus are DSELx, BWRITE, BWAIT, BTRAN [1:0], BPROT [1:0], BSIZE [1:0], BnRES, BLOK, BLAST, BERROR, BD[31:0], BCLK, BA[31:0], AREQx and AGNTx.

Advanced High Performance Bus (AHB)

AHB master helps in read and write operations through address and control. AHB system design may contain more than one master. At one time, only one of master can use the bus efficiently. AHB Slave responds to the AHB Master.

With the help of the address; slave responds to the read or writes operation. The status of the data transfer is acknowledged by the slave to the master. Status means whether the data transfer was a success, failure or a wait. AHB Arbiter and AHB Decoder have functions similar to ASB.

AHB signals are HWDATA [31:0],

HSELx, HRDATA [31:0],

HREADY, HRESP [1:0],

HSPLITx [15:0],

HMASTLOCK, HMASTER [3:0],

HGRANTx, HLOCKx and HBUSREQx.

AHB-Lite v1.0 supports a single master and provides a better bandwidth operation. Other than the basic AHB signals, this version uses other signals also; for better operation.

IV. SIMULATION RESULTS

The simulation is performed using Xilinx ISE 14.7 software.

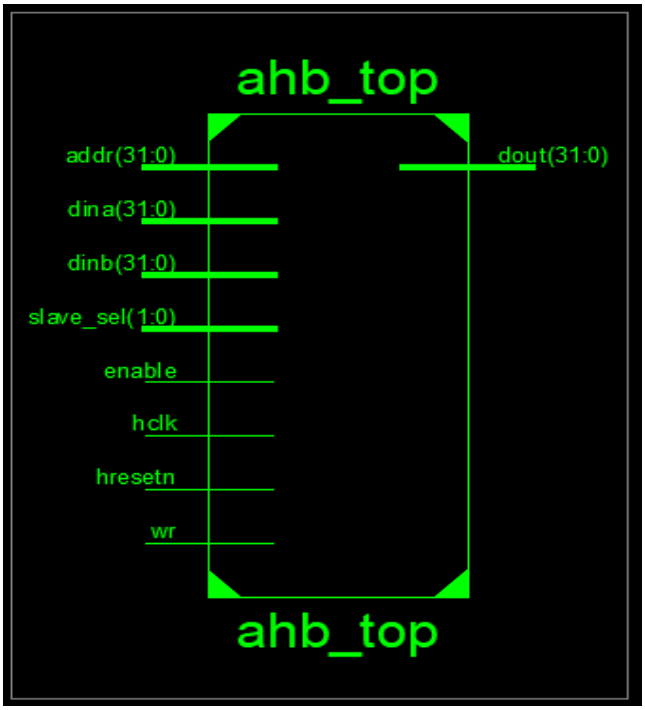

Figure 2: Top View

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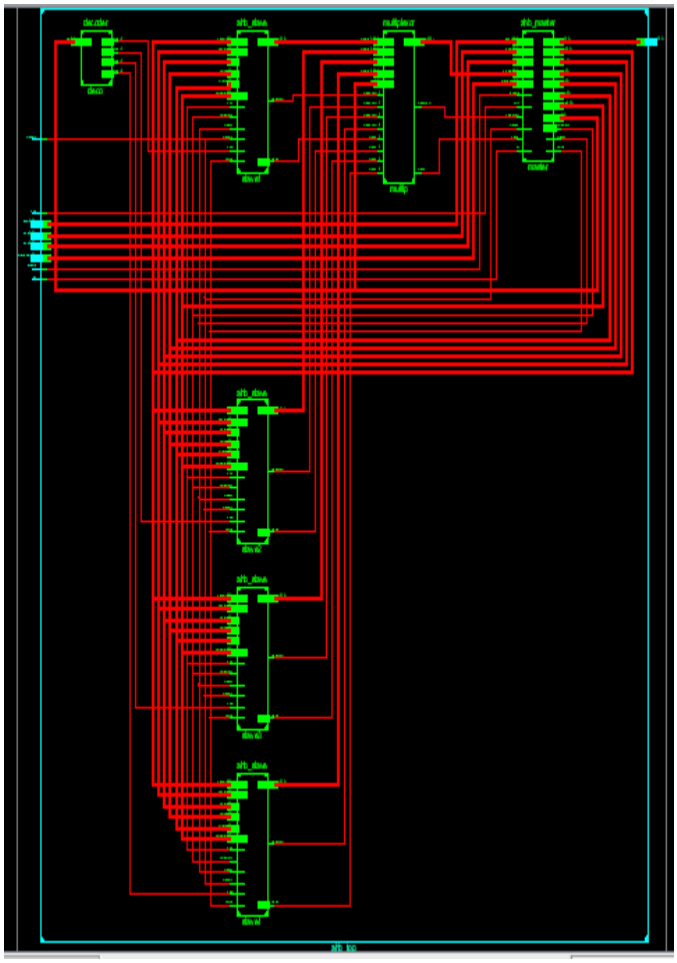

Figure 3: Complete RTL view

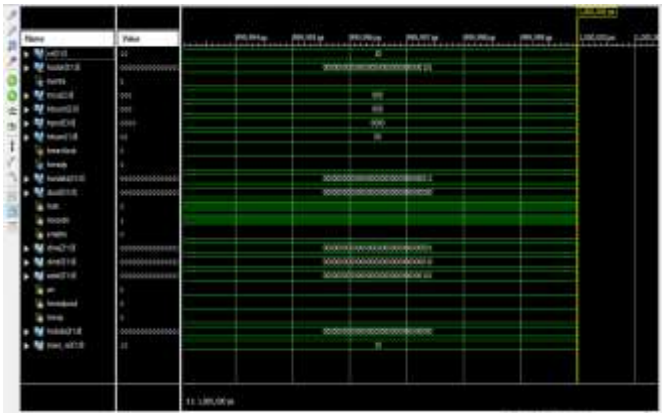

Figure 4: AHB master

Figure 5: AHB Top

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	242	408000	0%
Number of Slice LUTs	335	204000	0%
Number of fully used LUT-FF pairs	154	423	36%
Number of bonded IOBs	107	600	17%
Number of BUFG/BUFGCTRLs	1	32	3%

Figure 6: Device utilization summary

Table 1:
Simulation results

Sr no.	Parameter	Value
1	Area	11.2 %
2	Look up table	335
3	IOBs	107
4	BUF	1
5	Delay	0.57ns
6	Simulation time	32 sec
7	Memory	4654864 kilobytes
8	Frequency	754 MHz
9	Speed	2.4 Gbps
10	Power	0.8 mW
11	Global Fan out	100000

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V. CONCLUSION

The phenomenal growth of very large scale integration (VLSI) technology has made it possible to include millions of semiconductors onto a single chip, creating what is known as a system on chip (SoC). The AMBA-AHB Protocol for SoC Applications is designed and verified in its entirety as part of this process. AMBA Bus is made up of a great number of different parts, the most important of which are the AHB, ASB, and AXI, along with a number of other parts as well. AMBA Bus also includes a number of additional parts. These components are high-performance transports that are used to interact with low-performance execution transports such as APB. This paper presents VLSI implementation of Advanced Microcontroller Bus Architecture-Advanced High Performance Bus (AMBA-AHB) protocol. Simulation results show the significant improvement in the performance parameter with efficient design.

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