International Journal of Recent Development in Engineering and Technology
Website: www.ijrdet.com (ISSN 2347-6435(Online) Volume 12, Issue 01, January 2023)

A survey on Booth Multiplier with IOT Application

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***Abstract*—Various arithmetic operations such as multiplication addition, subtraction are important part of digital circuit to speed up the computation speed of processor. However the speed of processor greatly depends on multiplier unit of the processor. Different computer arithmetic techniques can be used to implement a digital multiplier. With advances in technology, many researchers have tried and are trying to design multipliers. This paper presents review of VLSI implementation of booth multiplier for FPGA-IOT applications.**

***Keywords*—FPGA-VLSI, IOT, Multiplier, Booth, Perfromnace, ALU.**

I. INTRODUCTION

Different computer arithmetic systems can be utilized to execute an advanced multiplier. Out of these most procedures include computing a lot of halfway products, and afterward adding the incomplete products together. Until the 1970s, most minicomputers didn't have increase guidance be that as it may, Centralized server PCs had duplicate guidelines, yet they did the a few sorts of movements and includes as an "increase schedule". Early chip additionally had no duplicate guidance. At that point the Motorola 6809, presented in 1978, was probably the most punctual microchip with devoted equipment increase guidance. It did likewise sorts of movements and includes as a "duplicate daily practice", yet the thing that matters is that execution was done in the microcode of the MUL guidance. As more transistors per chip got accessible because of bigger scale coordination, it got conceivable to put satisfactory adders on a single chip to total all the fractional products without a moment's delay, as opposed to reuse a single snake to deal with every halfway product each in turn. Presently, on the grounds that some normal advanced sign preparing algorithms invest the vast majority of their energy duplicating, computerized signal processor fashioners penance a great deal of chip area so as to make the increase as quick as would be prudent; a single cycle duplicate gather unit often spent the majority of the chip area of early DSPs. The development of most computerized frameworks is a huge assignment. Restrained creators in any field will subdivide the first undertaking into sensible subunits building squares and will utilize the standard subunits at every possible opportunity. In computerized equipment, the structure squares have such names as adders, registers, and multiplexers.

Different arithmetic activities, for example, duplication expansion, subtraction are significant piece of advanced circuit to accelerate the calculation speed of processor. Anyway the speed of processor enormously relies upon multiplier unit of the processor. This thusly expands the interest of rapid multiplier design in ALU and in different advanced sign processors. A few new multiplier engineering has been presented in the course of recent decades. Booth's multiplier [7] and modified booth's [12] multiplier are well known in current VLSI structure however they have their own arrangement of detriments. In this multiplier before showing up the last answer a few middle of the road steps are required that eases back the speed of processor. This middle of the road steps incorporates a few moving tasks, examination and subtraction which decrease the speed of processor exponentially as the quantity of bits present in multiplier and multiplicand increments. Since Speed is significant worry in creating processors now days, so new engineering must be presented which are quicker than previously mentioned multiplier. To address the previously mentioned hindrance of traditional multiplier booth's multiplier and modified booth's multiplier another engineering dependent on approximate multiplier is investigated.

In applications like interactive media signal preparing and information mining which can endure error, careful computing units are not constantly essential. They can be supplanted with their approximate partners. Research on approximate computing for error tolerant applications is on the ascent. Adders and multipliers structure the key segments in these applications. In approximate full adders are proposed at transistor level and they are used in advanced sign preparing applications. Their proposed full adders are utilized in aggregation of halfway products in multipliers.

To decrease equipment multifaceted nature of multipliers, truncation is generally utilized in fixed-width multiplier plans. At that point a steady or variable rectification term is added to make up for the quantization error presented by the shortened part. Estimation procedures in multipliers center around gathering of halfway products, which is vital regarding power utilization. Broken array multiplier is executed, where the least critical bits of sources of info are shortened, while shaping incomplete products to diminish equipment multifaceted nature.

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II. LITERATURE SURVEY

Y. -H. Chen et al.,[1] propose a data scaling technology (DST) for use in a low-error fixed-width Booth multiplier (FWBM) to reduce truncation errors. The proposed DST reduces the number of redundant bits in the multiplicand, yielding more efficient bits in low-error FWBMs. The truncation errors in FWBMs are reduced by adding a circuit incorporating the proposed DST to them as well as an error-compensation circuit. We found that the signal-to-noise ratio of the proposed DST-FWBM (1 bit) was more than 1.05 dB higher than that of an FWBM without the DST circuit. Long-width DST-FWBMs achieved an accuracy closely approaching the ideal value of a post-truncated multiplier. To verify its performance in a VLSI chip, we implemented the DST-FWBM in a 0.18-µm CMOS process. The proposed DST method was shown to considerably improve the accuracy of FWBMs, rendering this technology suitable for use in digital signal processing techniques.

P. Kavipriya et al.,[2] Multipliers are an essential part in DSP and VLSI design. Among conventional multipliers Booth multiplier is widely used. The aim of this work is to plan a Booth multiplier which can give better execution attributes, for example, rapid, low force, less area than the other regular multipliers. This work considers a Booth multiplier using a modified SQRT CSLA (Square Root Carry-select-adder). Modified SQRT CSLA is possible to incorporate by using BEC (Binary to excess one converter) or a CBL instead of a RCA (Ripple Carry Adder). CBL is most efficient when compared to BEC so CBL is preferred in designing a Booth multiplier.

H. Waris et al.,[3] The focus of existing designs on approximate radix-8 Booth multipliers has been on ASIC-based platforms. These multipliers are based on an approximation as defined for ASIC-based systems, so they cannot achieve comparable performance gains when used for FPGA-based hardware accelerators. This is due to the inherited architectural differences between FPGAs and ASICs. This brief bridges this gap by proposing high-performance approximate radix-8 Booth multipliers whose designs target FPGA-based systems. Hence, two approximate radix-8 Booth multipliers (referred to as AxBM1 and AxBM2) are proposed. Approximation is implemented such that the 6-input lookup table (LUT) and the associated carry chains of the FPGAs are fully utilized. AxBM2 exhibits 49% improvement in delay compared to the previous best FPGA-targeted design (Booth-Approx). AxBM2 has the advantage of complementing errors; this feature has been combined with truncation to achieve up to 60% in energy savings.

Moreover, the resolution of the previous state-of-the-art error-energy Pareto front is improved, such that better energy gains can be achieved for a given error constraint. As a case study, the proposed multipliers are applied to the application of Sobel edge detection, AxBM2 detected 98.45% edges with energy savings of 26.41%.

Y. -H. Chen et al.,[4] propose a data scaling technology (DST) for use in a low-error fixed-width Booth multiplier (FWBM) to reduce truncation errors. The proposed DST reduces the number of redundant bits in the multiplicand, yielding more efficient bits in low-error FWBMs. The truncation errors in FWBMs are reduced by adding a circuit incorporating the proposed DST to them as well as an error-compensation circuit. We found that the signal-to-noise ratio of the proposed DST-FWBM (1 bit) was more than 1.05 dB higher than that of an FWBM without the DST circuit. Long-width DST-FWBMs achieved an accuracy closely approaching the ideal value of a post-truncated multiplier. To verify its performance in a VLSI chip, we implemented the DST-FWBM in a 0.18-µm CMOS process. The proposed DST method was shown to considerably improve the accuracy of FWBMs, rendering this technology suitable for use in digital signal processing techniques.

P. K. Somayajulu et al.,[5] produces high power dissipation. As the technology shrinks to 65nm, there is no much increase in dynamic power dissipation but the leakage power increases tremendously. So there is a need for low power techniques to reduce the associated power. This power reduction can be obtained by system or algorithm or architectural level. Booth multiplier has wide application in low power VLSI. It is due its less computation time, low area and less power consumption. This work aims to design a pipelined 64 bit Booth multiplier. In the normal process of reduction of the partial products of binary of radix-16, the maximum height of the column of the partial products is n+1/4 where, n is the unsigned operand. The carry save adders are used for reducing height to n/4. The recoding of the booth multiplier is implemented. In this work carry save adder is replaced by the carry skip adder for reducing the power and area. The power consumption reduced by 11% and the area reduction obtained was 9%.

H. Waris et al.,[6] Radix-4 Booth encoding provides ease in the generation of partial products, thus is widely used to achieve power-efficient and low-area signed multipliers. Conversely, the radix-8 Booth encoding exhibits low-performance as it requires generation of odd multiples of the multiplicand.

In this brief, this issue is addressed by approximating the odd multiples of radix-8 to their nearest power of two such that the errors complement each other. In the pursuit of an accuracy-energy trade-off, hybrid low radix (HLR) based two approximate Booth multipliers (HLR-BM1 and HLR-BM2) are designed. HLR-BM2, compared to the previous best error-optimized design (ABM1), achieved a reduced energy of 22% with a comparable MRED. Moreover, HLR-BM2 achieves an improvement of 75% in MRED and 11% in energy consumption compared to the previously best energy-optimized design (RAD64). As a case study, performance for image transformation is evaluated. A high peak signal-to-noise ratio (PSNR, close to 50dB) is obtained for the proposed multiplier designs.

P. Patali et al.,[7] The performance of a digital signal processing (DSP) system is greatly affected by the performance of its multiplication operations. Simultaneous improvement in performance metrics such as delay, power, area, and energy efficiency is difficult to achieve and is a challenge to be addressed. To this end, an efficient carry save multiplier (CSM) that employs modified square root carry select adder (MSCA) for the vector-merging addition and improved full adder (IFA) in place of conventional full adder is proposed. Among 16x16 multipliers, the critical path delay (CPD), power, area, power delay product (PDP), and area delay product (ADP) of the proposed CSM are improved by 27.74, 19.4, 46.2, 41.4, and 60.87 percent respectively in comparison with improved booth multiplier and by 46.43, 31.46, 36.9, 63.05, and 65.96 percent respectively in comparison with low PDP booth multiplier. Cadence software with gpdk 45nm standard cell library is used for the design and implementation.

A. Sinha et al.,[8] Approximate computing has emerged as a promising technique to develop energy efficient design solutions for error-tolerant applications. Many research efforts have been directed towards proposing approximations in power-hungry multiplier circuits. In this brief, we have introduced two variants of a broken array approximate booth multiplier design called SIBAM with partial error correction through discarded sign bit addition. Experimental results show that up to 63% of energy savings can be achieved compared to accurate multipliers with Mean Relative Error Distance (MRED) constrained at 1.5%. Moreover, extensive analysis shows that the proposed design outperforms state-of-the-art multipliers with energy savings achievable up to 24% at 0.3% MRED constraint.

S. Venkatachalam et al.,[9] proposed approximate multipliers are demonstrated to have better performance than existing approximate Booth multipliers in terms of accuracy and power.

Compared to the exact Booth multiplier, ABM-M1 achieves up to a 23 percent reduction in area and 15 percent reduction in power with a Mean Relative Error Distance (MRED) value of 7:9 × 10 -4 . ABM-M2 has area and power savings of up to 51 and 46 percent respectively with a MRED of 2:7 × 10 -2 . ABM-M3 has area savings of up to 56 percent and power savings of up to 46 percent with a MRED of 3:4 × 10 -3 . The proposed designs are compared with the state-of-the-art existing multipliers and are found to outperform them in terms of area and power savings while maintaining high accuracy. The performance of the proposed designs is demonstrated using image transformation, matrix multiplication, and Finite Impulse Response (FIR) filtering applications.

W. Liu et al.,[10] approximate design of the RB-Normal Binary (NB) converter in the RB multiplier is also studied by considering the error characteristics of both the approximate Booth encoders and the RB compressors. Both approximate and exact regular partial product arrays are used in the approximate RB multipliers to meet different accuracy requirements. Error analysis and hardware simulation results are provided. The proposed approximate RB multipliers are compared with previous approximate Booth multipliers; the results show that the approximate RB multipliers are better than approximate NB Booth multipliers especially when the word size is large. Case studies of error-resilient applications are also presented to show the validity of the proposed designs.

D. J. M. Moss et al.,[11] present a two-speed, radix-4, serial-parallel multiplier for accelerating applications such as digital filters, artificial neural networks, and other machine learning algorithms. Our multiplier is a variant of the serial-parallel (SP) modified radix-4 Booth multiplier that adds only the nonzero Booth encodings and skips over the zero operations, making the latency dependent on the multiplier value. Two subcircuits with different critical paths are utilized so that throughput and latency are improved for a subset of multiplier values. The multiplier is evaluated on an Intel Cyclone V field-programmable gate array against standard parallel-parallel and SP multipliers across four different process-voltage-temperature corners. We show that for bit widths of 32 and 64, our optimizations can result in a 1.42×-$3.36× improvement over the standard parallel Booth multiplier in terms of area-time depending on the input set.

S. F. Sultana et al.,[12] propose a new way of implementing Fast Fourier transform multiplier. Previous approaches achieve FFTs with a unity gain using a complex multiplier or a non-unity gain factor. The IEEE 754 format is used for a floating-point number representation.

This project proposes an effective float reconstruction scheme that showed greater delay and area implementation. A community of Karatsuba and Urdhva-Tiryagbhyam algorithms is used to implement a binary multiplier. The algorithms are implemented by Verilog (HDL) and are targeted to the Xilinx ISE simulator for FPGA Spartan-3E board. This decreases the FFT architecture and design computing resources.

III. Challenges

There are some challenges into the booth digital multiplication, which is as followings-

- Implemented only 16 and 32 bit digital booth multiplier while the advance processor uses 64 bit operations.
- Ultra large scale integration is most advanced technology in the fabrication of integrated circuits. More than ten lakh components are integrated together in a single chip. More area size required for implementations by the existing research.
- Due to widespread application of portable electronic devices and the evaluation of microelectronic technology, power dissipation has become a critical parameter in low power VLSI circuit designs. In emerging VLSI technology, the circuit complexity and high speed imply significant increase in the power consumption.
- The network latency is an estimate of the delay of the clock tree before clock tree synthesis. After clock tree synthesis, the total clock latency from the clock source to a clock in of a flip flop is the source latency plus actual delay of the clock tree from the clock definition point to the flip flop. More delay or response time by existing research.

IV. Conclusion

This paper presents review of the low latency VLSI implementation of booth multiplier for FPGA-IOT applications. Various parameters analysis is studied like power, area, latency, throughput, frequency and power delay product to identify the improved architectures for high speed applications in previous research work. The proposed multiplier plans can be utilized in applications with negligible misfortune in yield quality while sparing huge power and area. The 64-bit inputs binary and hexadecimal will be given and 128 bit multiplier output will be resultant.

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