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Review of Advanced Microcontroller Bus Architecture Protocol for VLSI Application

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***Abstract*— The immense advancement of VLSI innovation empowers the coordination of millions of semiconductors on a solitary chip called System on chip (SoC). The absolute Design and Verification of AMBA APB Protocol for SoC Applications are performed. AMBA Bus essentially has a large number of components like AHB, ASB and AXI, and so forth which are elite transports used to interface with low-performance execution transports like APB. APB uses low peripheral bandwidth and is used to connect with slaves like UART, timer, keypad and interrupt controller etc. This paper presents the review of advanced microcontroller bus architecture protocol for VLSI application.**

***Keywords*—AMBA, APB, AXI, AHB, VLSI, Microcontroller.**

I. INTRODUCTION

AMBA was introduced by ARM in 1996. The first AMBA buses were the Advanced System Bus (ASB) and the Advanced Peripheral Bus (APB). In its second version, AMBA 2 in 1999, ARM added AMBA High-performance Bus (AHB) that is a single clock-edge protocol. In 2003, ARM introduced the third generation, AMBA 3, including Advanced eXtensible Interface (AXI) to reach even higher performance interconnect and the Advanced Trace Bus (ATB) as part of the CoreSight on-chip debug and trace solution.

Advanced Peripheral Bus (APB) is the piece of Advanced Microcontroller Bus Architecture (AMBA) family conventions. It is an easy interface and the arrangement is to improve the plan for the least possible power intake and diminished interface unpredictability. In contrast to AHB, it is a Non-Pipelined convention, used to associate low-data transfer capacity peripherals to the SoC [1]. The Advanced Microcontroller Bus Architecture (AMBA) offering from ARM is one of the most widely used standards for System on Chip (SoC) design in the semiconductor industry. The specifications defined by AMBA provide many advantages such as right-first-time development and technology independence for design of high performance chipsets [2]. In today's era AMBA (advanced microcontroller bus architecture) specifications have gone far beyond the Microcontrollers.

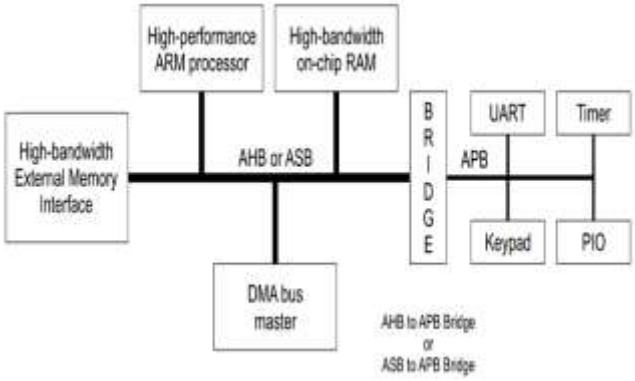

Figure 1: AMBA

In this work, AMBA (Advanced Microcontroller Bus Architecture) ASB APB (Advanced system bus - Advanced Peripheral Bus) is implemented. The goal of the proposed work is to synthesis, simulate complex interface between AMBA ASB and APB. The methodology adopted for the proposed work is Verilog language with finite state machine models designed in ModelSim Version 10.3 and Xilinx-ISE design suite, version 13.4 is used to extract synthesis, design utilization summary and power reports. For the implementation APB Bridge, arbiter and decoder are designed. In AMBA ASB APB module, master gets into contact with APB bus. Arbiter determines master's status and priority and then, starts communicating with the bus [6].

II. LITERATURE SURVEY

P. Jain et al.,[1] present work is to plan and examine the different functional aspect of the protocol. i.e. information read from a specific system area is the similar as the information written to the given system area and the protocol verifies the functionality by passing random value to same indexed address, random value for randomly indexed address and grouping write and read values together. The system embraced for the proposed work uses Verilog language and Verilog Testbench to extract synthesis, design usage synopsis.

The design utilized Verilog programming which greatly enhances reusability of the Testbench components such as creating Tasks for various Test cases.

A. Suresh et al.,[2] The main focus in this work is on two protocols - Advanced Highperformance Bus (AHB) and Advanced peripheral Bus (APB). Keeping in mind that these specifications are an open standard, we aim to develop an AMBA AHB-APB bridge from Register Transfer Level (RTL) to Graphical Display System (GDSII) using only open source tools and libraries. The proposed design is developed with Verilog Hardware Definition Language (HDL), followed by compilation and functional simulation. Physical design is performed after verification to obtain graphical display of the bridge module. Detailed analysis of the results obtained indicates that open source options are viable to test various digital designs obviating the need to invest in expensive proprietary design tools. This would accrue benefit by greatly improving the scope and reach of Very Large Scale Integration (VLSI) design.

N. Gaikwad et al.,[3] In the ever changing world where every day new IPs and chips are designed with less time to market, creating a very robust verification mechanism within a short duration is a big need of fast growing VLSI industry. With the advent of a standardized signal bus architecture used for interconnection of various modules of a system, system-on-a-Chip (SoC) design became the major integrated methodology for minimizing the design time of complete system. Now how to verify these on chip bus protocols is one of the grave challenges at hand, also traditional methods are inefficient for verifying large SoC. In this work we have built a verification environment for AXI protocol using System Verilog (SV) where we had verified AMBA AXI Protocol achieving successful Write and Read Operations for incrementing burst feature with a saleable test bench architecture.

K. Rudnicki et al.,[4] present an IP core of coprocessor supporting computations requiring integer multiple-precision arithmetic (MPA). Whilst standard 32/64-bit arithmetic is sufficient to solve many computing problems, there are still applications that require higher numerical precision. Hence, the purpose of the developed coprocessor is to support and offload central processing unit (CPU) in such computations. The developed digital circuit of the coprocessor works with integer numbers of precision approaching maximally 32 kbits. Our IP core is developed using the very high speed integrated circuit hardware description language (VHDL) and simulated assuming implementation in field-programmable gate arrays (FPGAs).

It exchanges data using three 64-bit data buses whereas a code for execution on the coprocessor is fetched from a dedicated 8-bit bus (all buses in AMBA standard - AXI Stream). An instruction set of the coprocessor currently consists of 7 instructions including multiplication, addition and subtraction. The computations can maximally employ 16 registers of the length 32k bits. Simulation results assuming implementation on Zynq system on chip (SoC) show that computations of the factorial (n!) for n=1000 take 326.4 μsec. Such a design currently requires 7982 look-up tables (LUTs), 10400 flip-flops (FFs), 33 block RAMs (BRAMs) and 28 DSP modules. The processor is aimed to provide scalability allowing one to use the developed IP core not only in scientific computing, but also in embedded systems employing encryption based on MPA.

N. Pravin et al.,[5] This work presents a Field Programmable Gate Array (FPGA) based implementation of the Fourier Segmentation process that is used in the Empirical Wavelet Transform. The Empirical Wavelet Transform is a method to determine the modes of a given signal by building wavelets that are adapted to the processed signal. Such wavelets are constructed by determining the location of the information in the spectrum of the signal and hence, the segmentation of the Fourier spectrum plays a crucial role in extracting the modes of the signal. However, the Fourier segmentation process is a time consuming process making it difficult to reach real-time constraints. The proposed design aims to addresses this issue. It utilizes the AMBA AXI-4 STREAM protocol for inter-module communication. The design has been simulated to test its functionality using the Xilinx Vivado Simulator and verified by implementation in Xilinx Virtex-7 XC7VX690T FPGA.

K. Rawat et al.,[6] For selecting a bus slave, decoder uses the accurate address lines and an acknowledgement is given back to the bus master by the slave. An RTL view and an extracted design summary of AMBA ASB APB module at system on chip are shown in result section of the work. Higher design complexities of SoCs architectures introduce the power consumption into picture. The various power components contribute in the power consumptions which are extracted by the power reports. So, power reports generate a better understanding of the power utilization to the designers. These are clocks total power which consumes of 0.66 mW, hierarchy total power which consumes of 1.05 mW, hierarchy total logical power which consumes of 0.30 mW and hierarchy total signal power which consumes of 0.74 mW powers in the proposed design. Graph is also plotted for clear understanding of the breakdown of powers.

J. Chhikara et al.,[7] All design unit consists of smaller functional blocks called subsystems or module. For effective functioning of the system these modules need to be in sync with each other and share re-sources. Problem starts when one subsystem follows different protocol as others. Each module has its different bit rate or baud rate of data transfer which can be either asynchronous or synchronous. The work describes an architecture which defines how to transfer the data from one protocol to another protocol. It exploits the flexible protocols of I2C which makes it compatible with APB AMBA protocol. The proposed architecture is a bridge between I2C Master and APB Salve and can transfer data from I2C supported module to APB supported module and vice-versa. The data travels from a serial bus (I2C) to parallel bus (APB) to serial (I2C) in sync with the respective domain clock. This forms a bidirectional interface between I2C supported module and APB supported module.

K. Rawat et al.,[8] In this work, one of AMBA (Advanced Microcontroller Bus Architecture) known as AMBA APB (Advanced Peripheral Bus) is designed which provides minimum power consumption and low bandwidth. For this, an APB Bridge with Reset Controller design has been implemented in Verilog language. Reset controller introduces a reset signal BnRES during Power-on Reset (POReset) conditions so that propagation of metastable values can be eliminated and glitches can be avoided. Power report shows that the various power components contribute in the total power consumption by APB bridge architecture. As the result of this work: Bridge under POReset conditions, On-chip total power consumption is 9.52%, Hierarchy power consumption is 29.12% and dynamic supply power consumption is 28.89% less than Bridge under no PORset conditions. Hence, Bridge can be providing efficient utilization of power when it is designed under Power-on Reset conditions.

E. Karimi et al.,[9] present a new fault model for testing standard On-Chip buses using a graph model. This method will be optimized for speed of testing. Using AMBA-AHB as the experimental result, the proposed fault model shows efficiency in comparison with corresponding stuck-at fault testing.

Cheng-Ta Wu et al.,[10] As the design of SoC is getting more and more complicated, the IPs (Intellectual Property) reuse ability increasing is the key issue to improve the time of the embedded systems development and integration. However, the different SoC design environment will affect the IPs reuse ability, such as in different system bus. In this work we have implemented a standard OCP-AHB bus wrapper.

By this wrapper, the IP with OCP interface can connect to AMBA 2.0 AHB bus quickly, and IP designer can focus on the development of IP functionalities without considering the data transaction in different interconnects. This will reduce the IPs development time, and increase the reuse ability. Thus the system integration and verification can be accelerated. Furthermore, we added the built-in ICE architecture to make the SoC verification more flexible and quickly.

J. Cao et al.,[11] Simulators play an important role in the design of VLSI circuits, but they require a large investment of time and effort. In this work we present a high-level, Markov model of a protocol, and we show how the best performing design can be selected without the need for simulation. Novel is the way we model the combinational logic and buffers as separate components. We compute the power consumed by each component, as well as the area complexity and data throughput. As a case study, we formally model the industrial protocol AMBA, and generate 84 designs that fulfil certain correctness requirements. We predict the performance and area complexity of every design, and we compare our predictions with the results from simulation. A fidelity and linear regression analysis is used to compute the correlation between the predictions and simulations. We also consider the competing goals of low-power and high-throughput, and how to select a design that offers an optimal compromise.

R. Wang et al.,[12] presents a physical synthesis scheme for on-chip buses and bus matrices to minimize the power consumption, without changing the interface or arbitration protocols. By using a bus gating technique, data transactions can take shortest paths on chip, reducing the power consumption of bus wires to minimal. Routing resource and bandwidth capacity are also optimized by the construction of a shortest-path Steiner graph, wire sharing among multiple data transactions, and wire reduction heuristics on the Steiner graph. Experiments indicate that the gated bus from our synthesis flow can save more than 90% dynamic power on average data transactions in current AMBA bus systems, which is about 5-10% of total SoC power consumption, based on comparable amount of chip area and routing resources.

III. Application

AMBA is widely used in a range of ASIC and SoC parts. These parts include applications processors that are used in devices like IoT subsystems, smartphones, and networking SoCs.

APB involves low bandwidth, low cost and minimal power consumption and is used to connect the Timer, Keypad and other devices to the bus architecture.

IV. CONCLUSION

The tremendous development of very large scale integration (VLSI) technology enables the integration of millions of semiconductors into a single chip, which is referred to as a system on chip (SoC). The Design and Verification of the AMBA APB Protocol for SoC Applications are carried out in their entirety. AMBA Bus is comprised of a vast number of components, the most notable of which are AHB, ASB, and AXI, as well as a number of others. These components are high-performance transports that are used to interface with low-performance execution transports, such as APB. A limited amount of peripheral bandwidth is utilised by APB, and it is used to communicate with slaves such as UART, timers, keypads, and interrupt controllers, among other things. In this study, an overview of sophisticated microcontroller bus architecture protocol for VLSI applications is presented.

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